

Compal Confidential

Q5WV8 Schematics Document

AMD "Comal" Platform

AMD Trinity APU / Hudson M3 FCH / ATI Thames XT

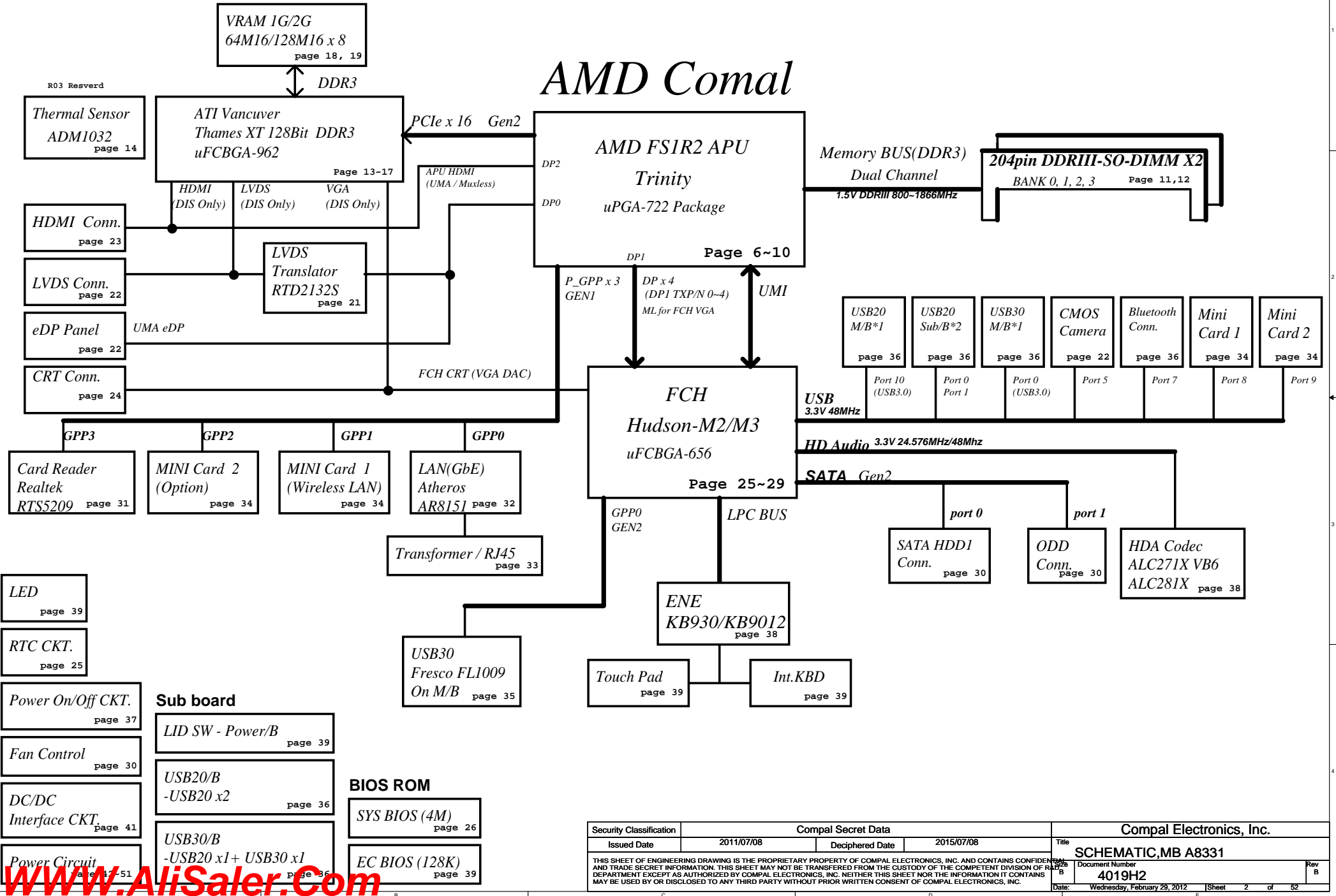
2012-01-05A

LA-8331P REV: 0.4

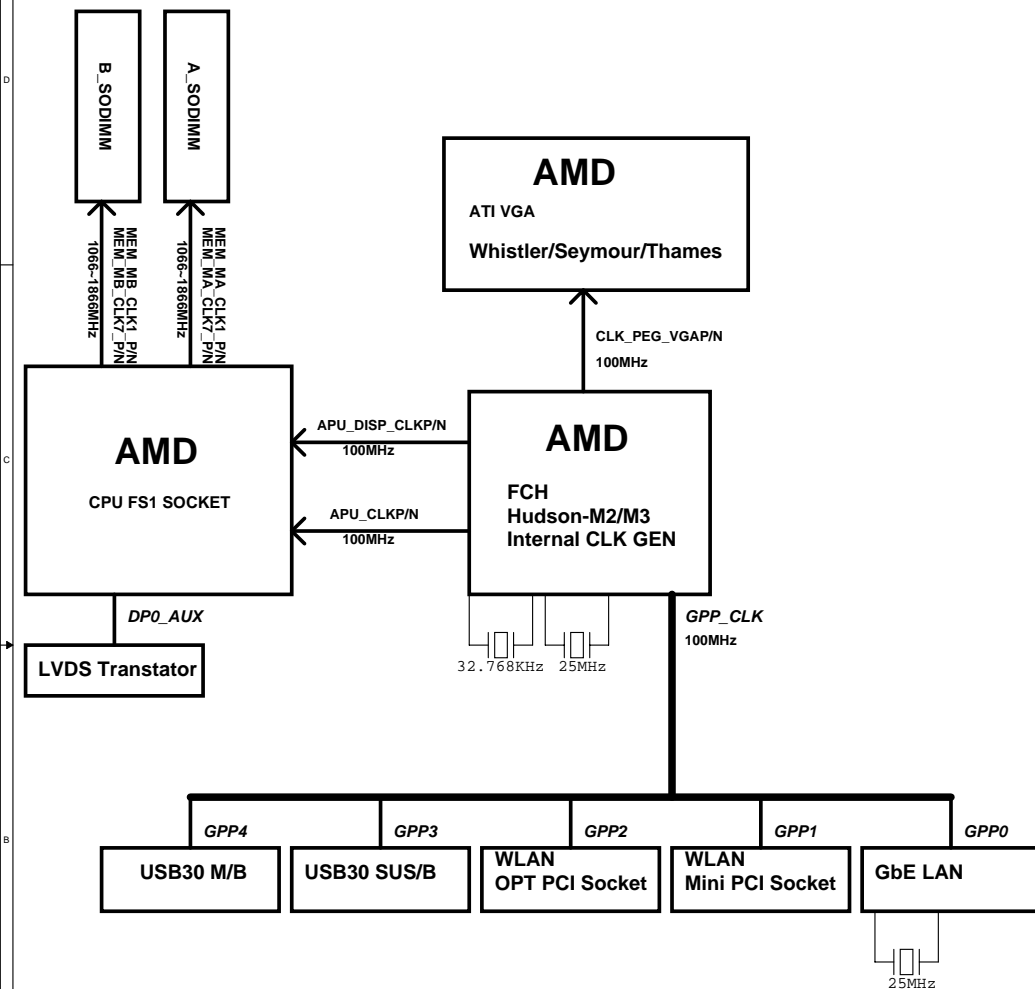
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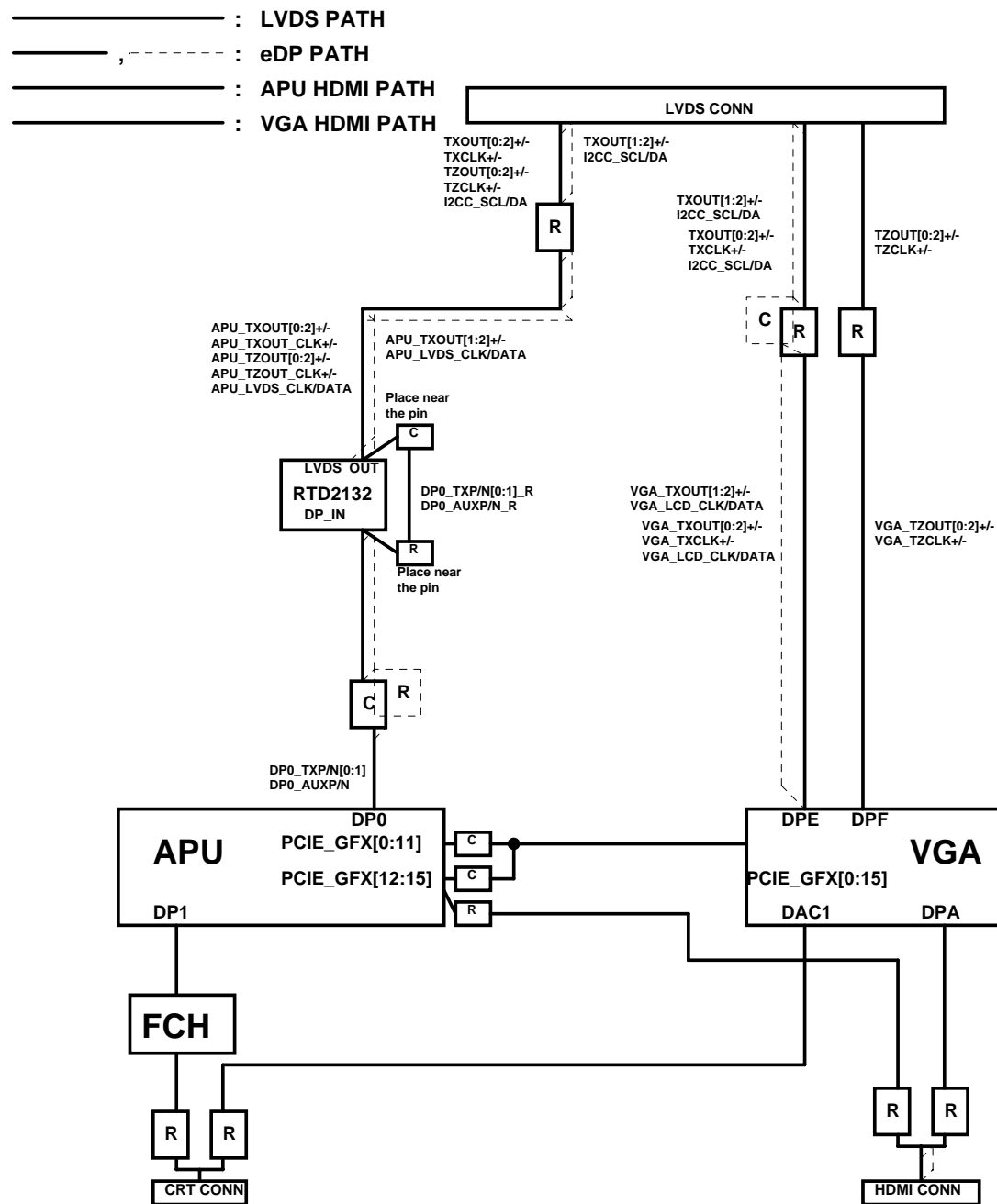
Model Name : Q5WV8



CLOCK DISTRIBUTION



DISPLAY DISTRIBUTION



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+CPU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+VDDCI	0.95-1.2V switched power rail	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	ON	OFF
+1.0VSG	1.0V switched power rail for VGA	ON	OFF	OFF
+1.1ALW	1.1V switched power rail for FCH	ON	ON	ON*
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF
+1.2VS	1.2V switched power rail for APU	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VSG	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

x = 1 is read cmd, x= 0 is write cmd.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

EC SM Bus2 address

Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	ADI ADM1032 (VGA)	1001 101X b	9AH
			SB-TSI (APU)	1001 100X b	98H
			LVDS TR(RTD-2132S)	1010 100X b	A8H
			VGA Internal Thermal	1000 001X b	82H

FCH SM Bus 0 address

FCH SM Bus 1 address

Device	Address	HEX	Device	Address	HEX
DDR DIMM1	1101 000X b	90			
DDR DIMM2	1101 001X b	94			

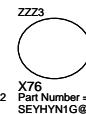
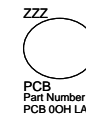
STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOM Option Table

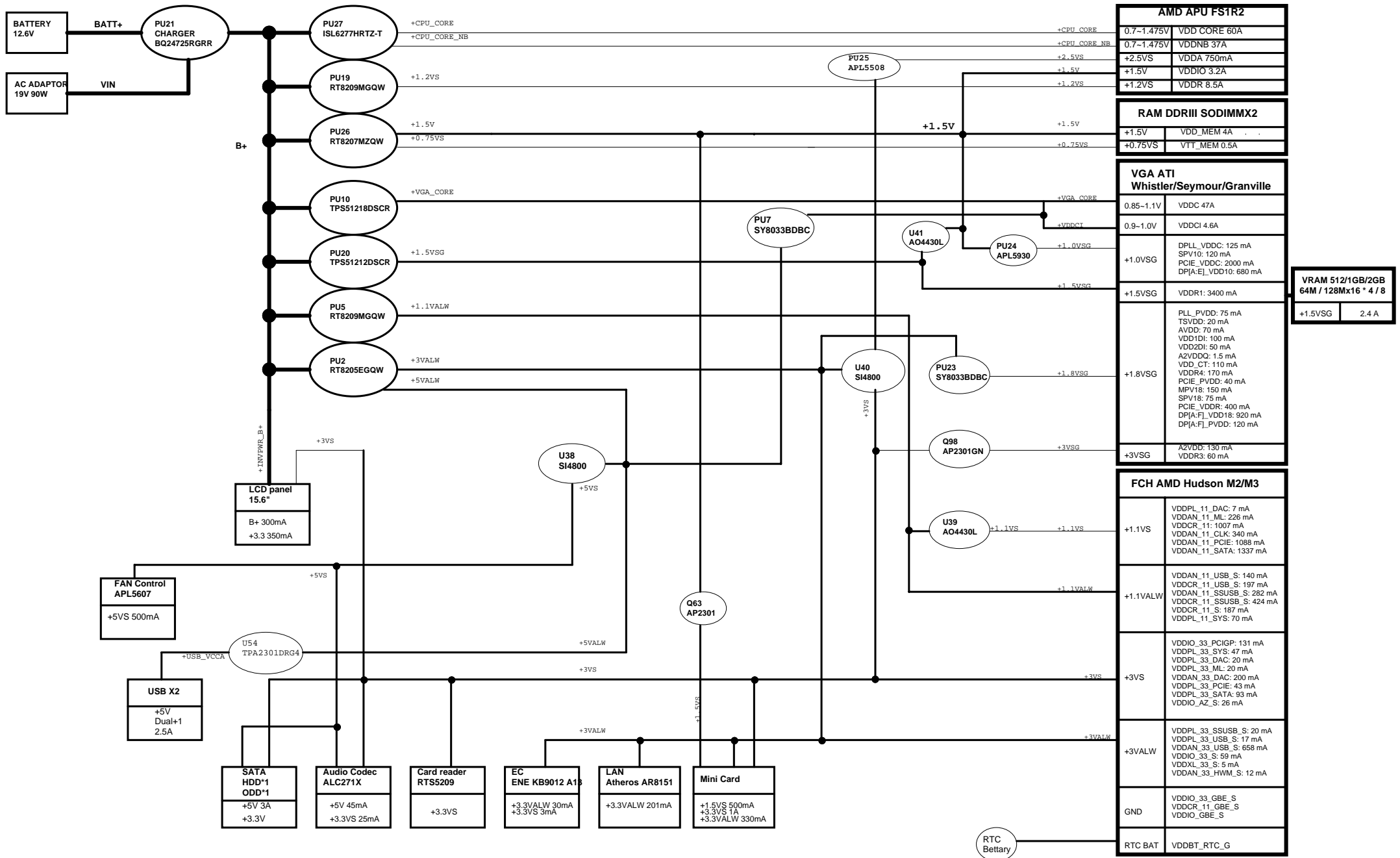
BOM Structure	Description	UMA	Thames	EVT2 UMA	DVT UMA-LVDS	DVT UMA-eDP	DVT PX5 1G-LVDS	DVT PX5 1G-eDP	DVT PX5 2G-LVDS	
M2@	Use Hudson-M2			V						
M3@	Use Hudson-M3	V	V		V	V	V	V	V	
930@	Use EC 930	V	V							
9012@	Use EC 9012			V	V	V	V	V	V	
UMA@	Display output from APU (UMA only or PX)	V	V	V	V	V	V	V	V	
DISO@	Display output from VGA (DIS only)									
VGALVDS@	VGA output LVDS (DIS only)									
VGA@	Use VGA (PX or DIS only)		V				V	V	V	
THA@	VGA: Thames		V				V	V	V	
SEY@	VGA: Seymour									
128@	Use VRAM channel A&B		V				V	V	V	
PX@	PX function		V				V	V	V	
BACO@	BACO function (PX4.0)		V							
NOBACO@	Without BACO function (DISO and PX5.0)						V	V	V	
TL@	LVDS Translator (for LVDS)	V	V	V	V		V		V	
EDP@	Use eDP Panel					V		V		
APUEDP@	APU output eDP					V		V		
VGAEDP@	VGA output eDP (DIS only)									
271@	Realtek ALC271x VB6	V	V	V	V	V	V	V	V	
281@	Realtek ALC281x									
ZERO@	ZERO Power ODD function									
FL@	Fresco FL1009 USB3.0 Controller			V						
8151@	LAN Atheros AR8151 10/100/1000M LAN			V	V	V	V	V	V	
8152@	LAN Atheros AR8152 10/100M LAN									
X76@	VRAM ID Table (Load By X76J)									
CONN@	Connector (Control by ME)									

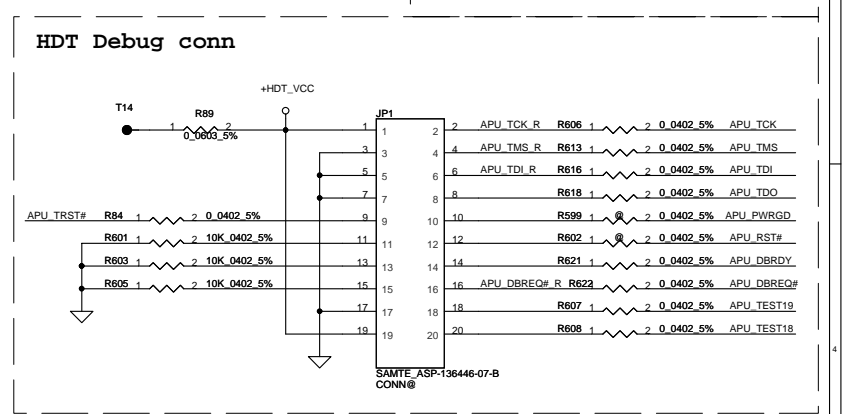
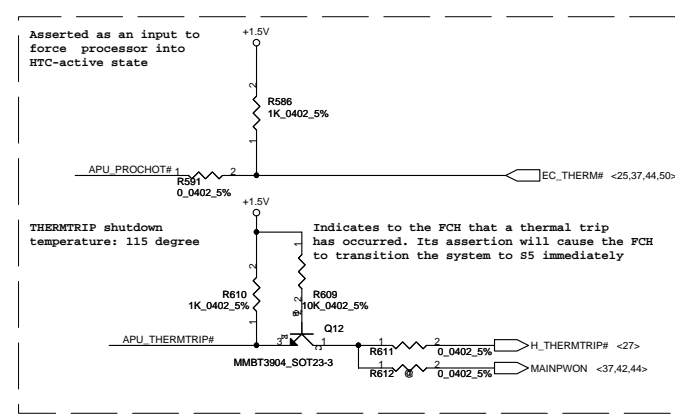
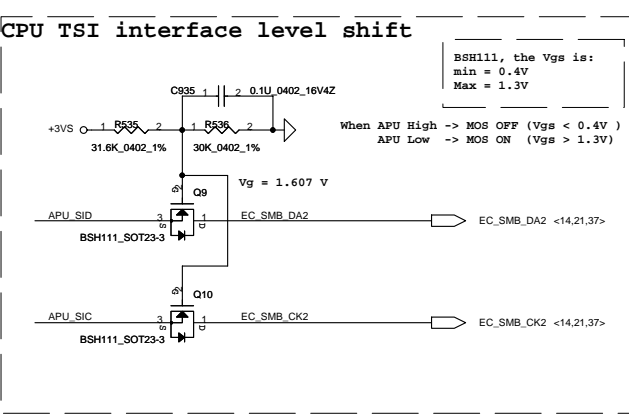
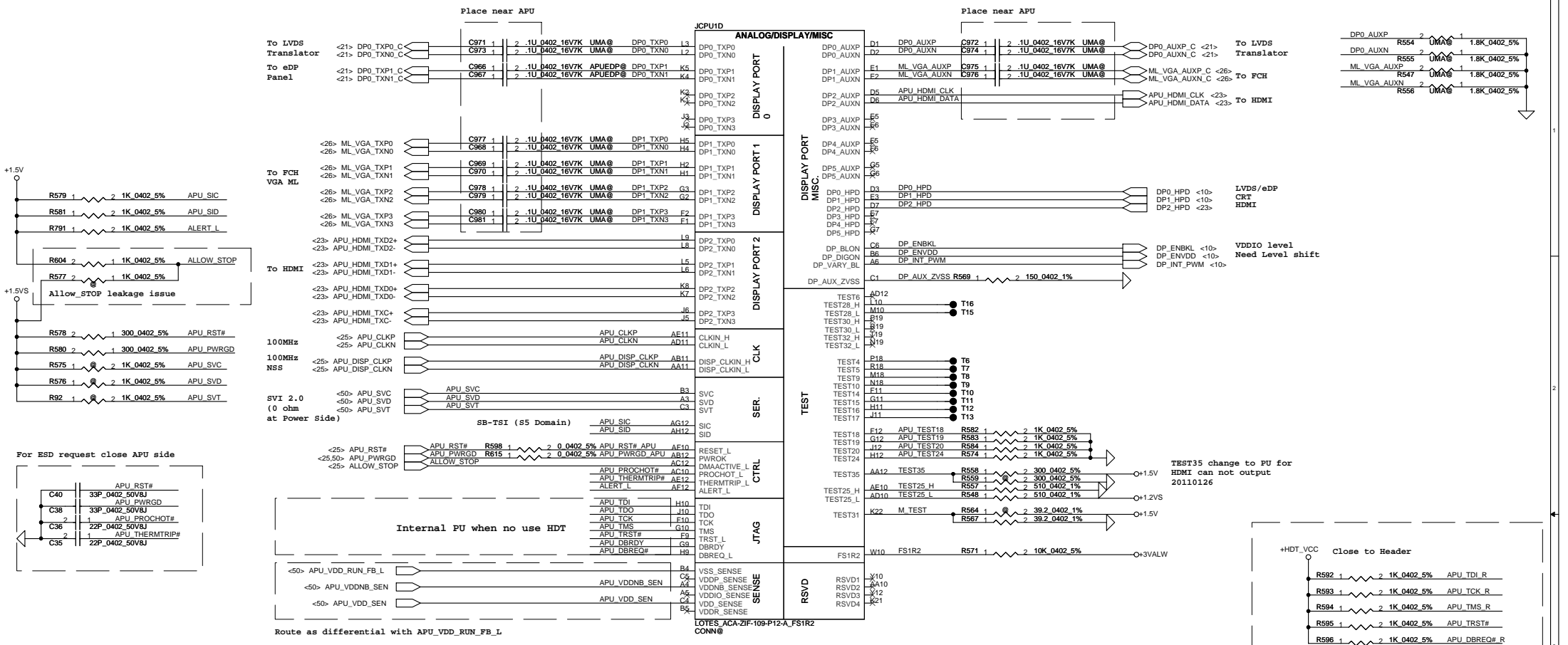


BOARD ID Table

Board ID	PCB Revision
0	EVT
1	EVT2
2	DVT
3	
4	
5	
6	
7	

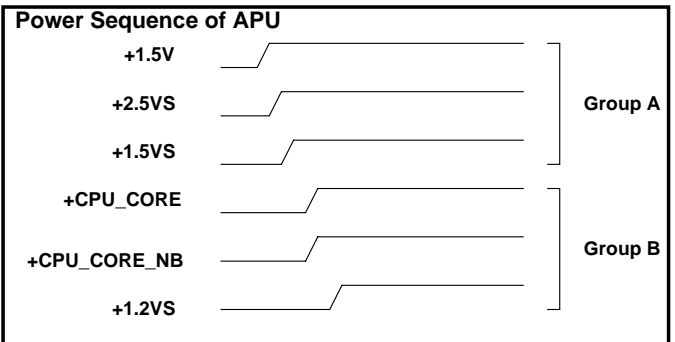
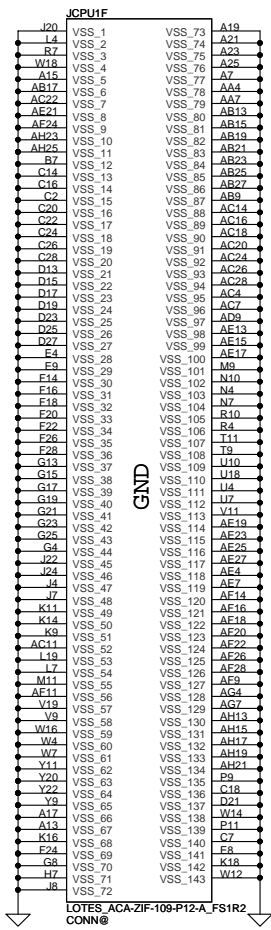
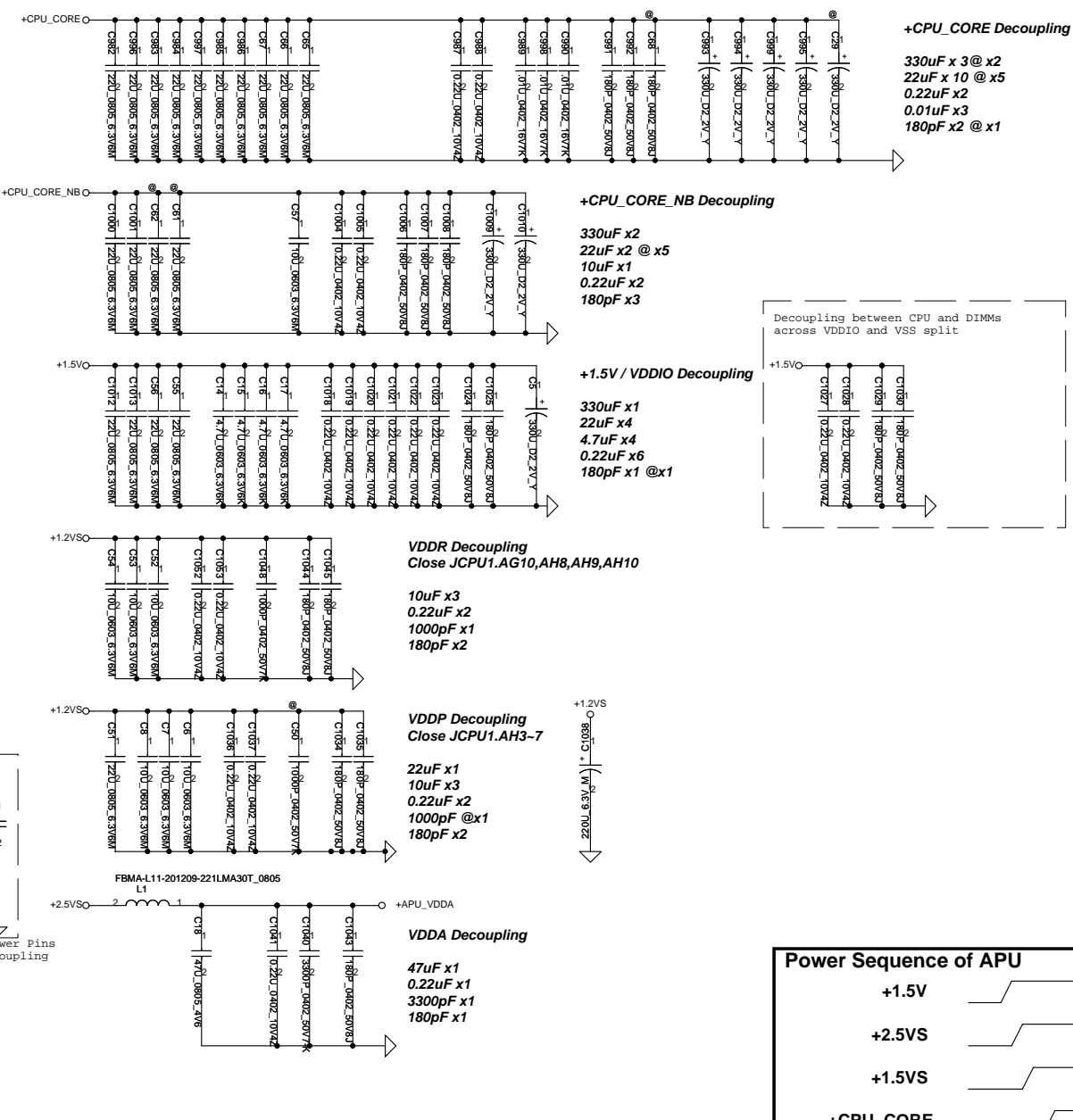
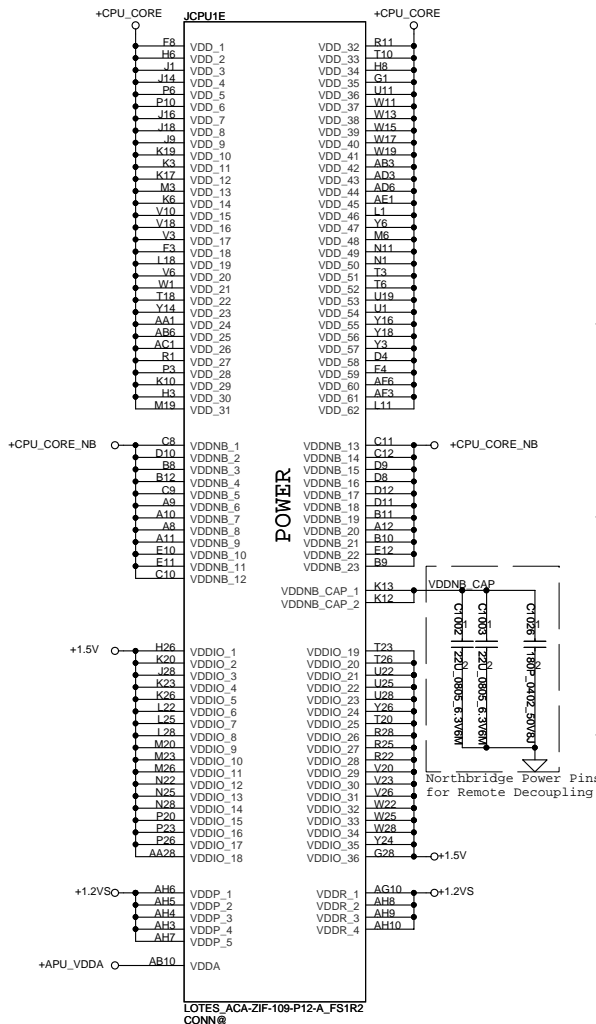
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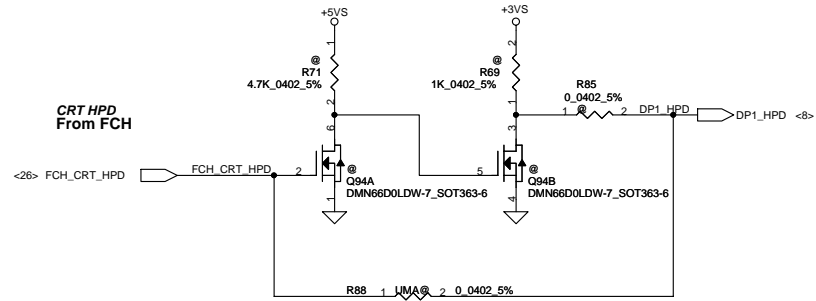
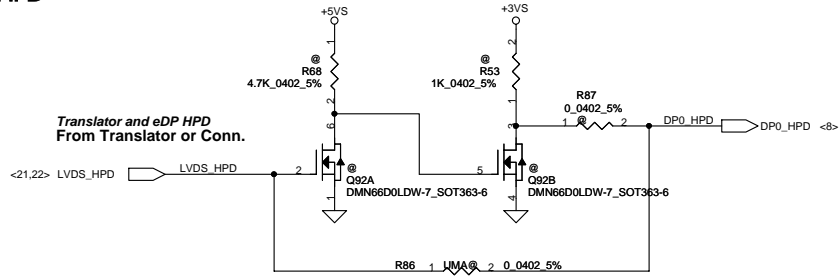
Power Name	Consumption
VDD +CPU_CORE	60A
VDDNB +CPU_CORE_NB	37A
VDDIO	3.2A
VDDP / VDDR +1.2VS	5A / 3.5A
VDDA +2.5VS	0.75A



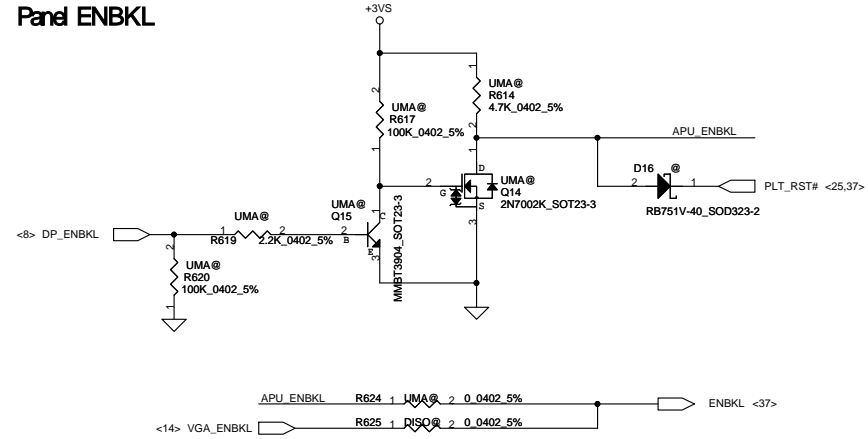
Decoupling Caps.									
Pop / @	330uF	220uF	47uF	22uF	10uF	4.7uF	0.22uF	0.01uF	3300pF
Pumori 2.0		0	19/11	7	5	17	3	1	1 / 1
Comal	7 / 2	1	1	19/11	7	4	17	3	1 / 1
P5WS5	7 / 2	1	1	13	3	8	19	3	1

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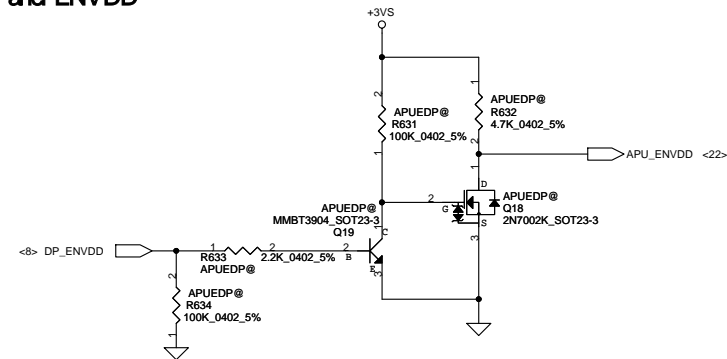
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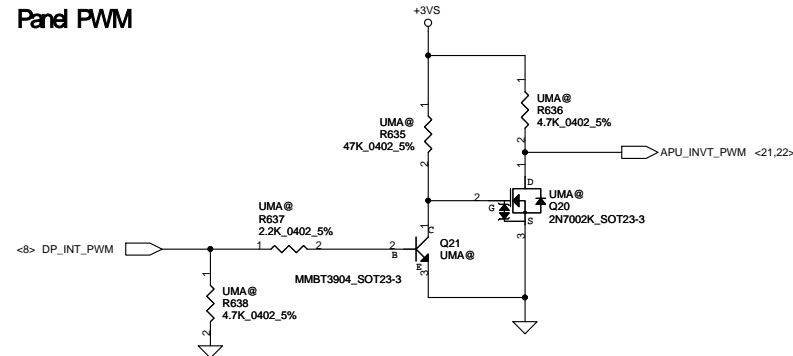
Panel ENBKL



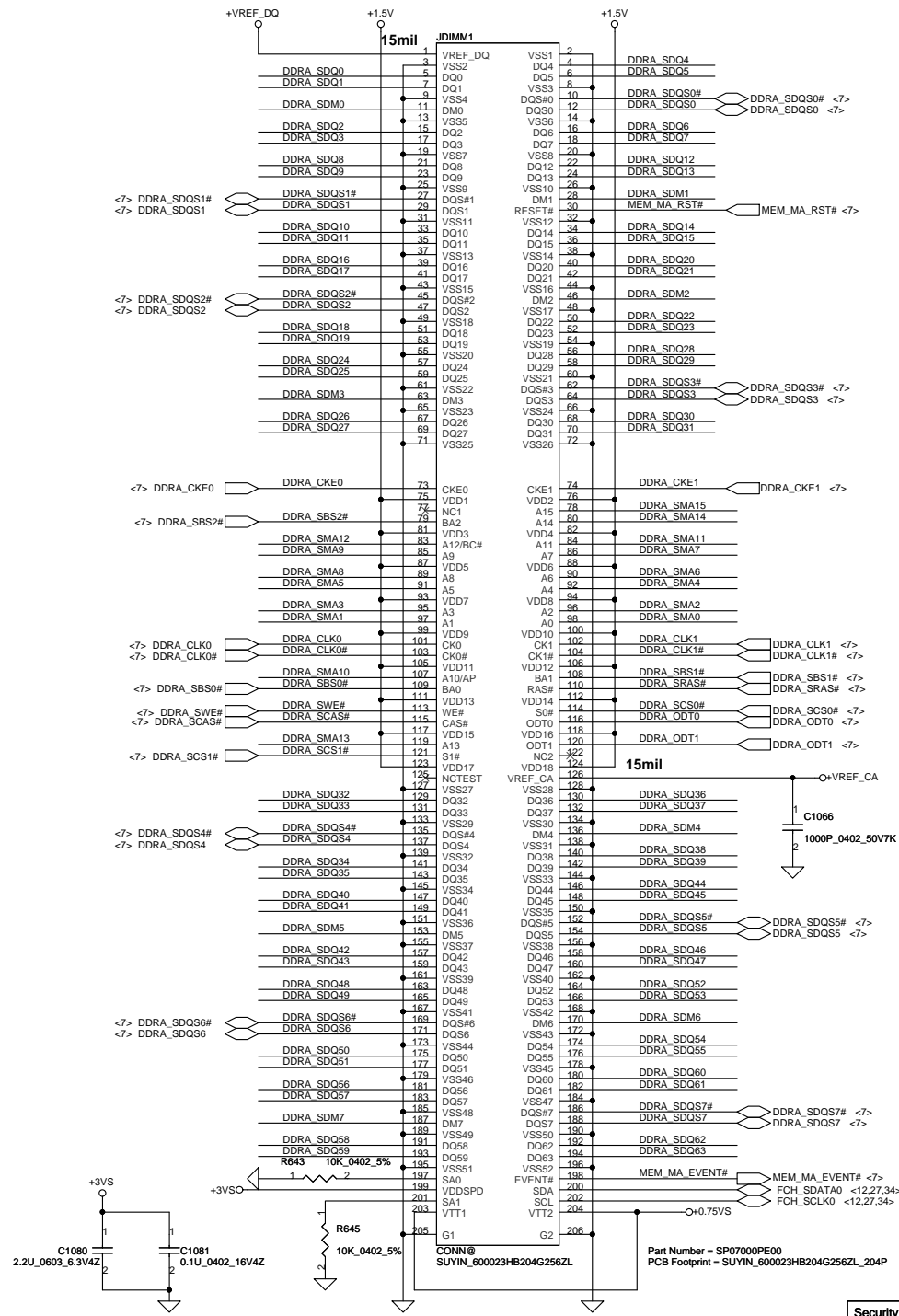
Panel ENVDD



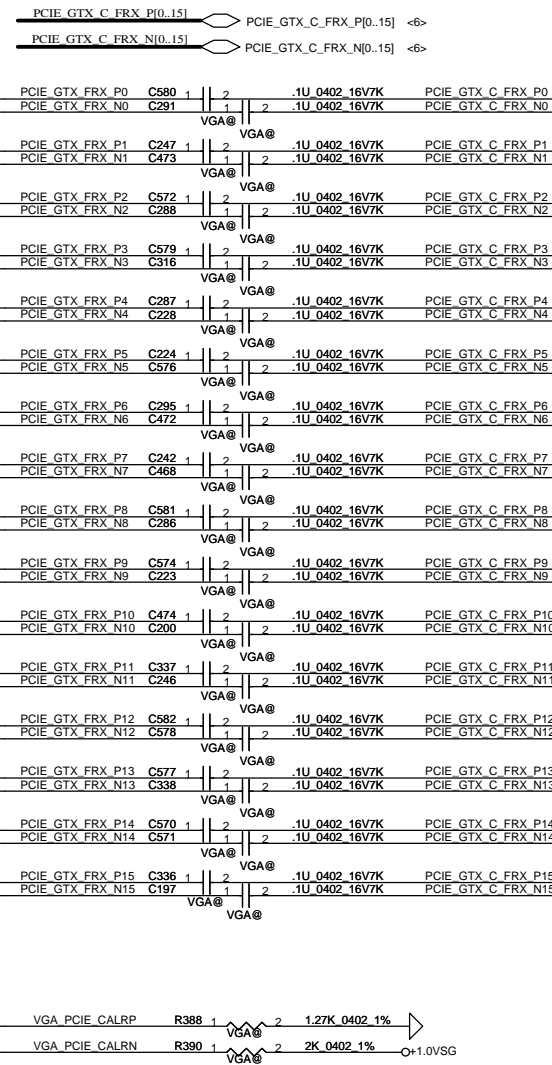
Panel PWM



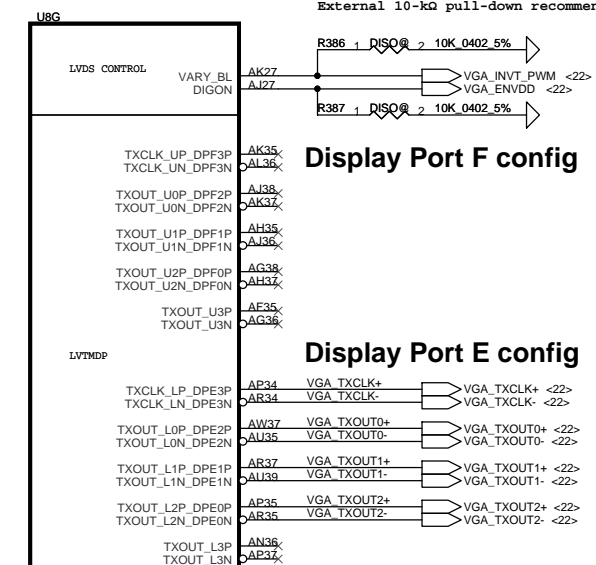
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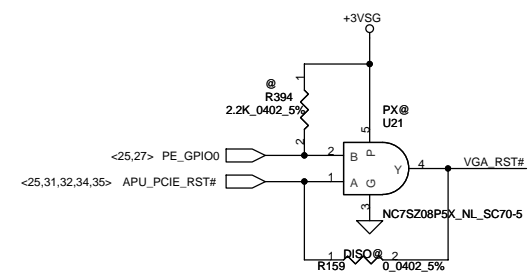
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<6> PCIE_FTX_C_GRX_N[0..15]	PCIE_FTX_C_GRX_N[0..15]		
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	PCIE_FTX_C_GRX_P1 Y35 PCIE_FTX_C_GRX_N1 W36	PCIE_RX1P PCIE_RX1N	PCIE_TX1P PCIE_TX1N
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	PCIE_FTX_C_GRX_P3 V35 PCIE_FTX_C_GRX_N3 U36	PCIE_RX3P PCIE_RX3N	PCIE_TX3P PCIE_TX3N
	PCIE_FTX_C_GRX_P4 U38 PCIE_FTX_C_GRX_N4 T37	PCIE_RX4P PCIE_RX4N	PCIE_TX4P PCIE_TX4N
	PCIE_FTX_C_GRX_P5 T35 PCIE_FTX_C_GRX_N5 R36	PCIE_RX5P PCIE_RX5N	PCIE_TX5P PCIE_TX5N
	PCIE_FTX_C_GRX_P6 R38 PCIE_FTX_C_GRX_N6 P37	PCIE_RX6P PCIE_RX6N	PCIE_TX6P PCIE_TX6N
	PCIE_FTX_C_GRX_P7 P35 PCIE_FTX_C_GRX_N7 N36	PCIE_RX7P PCIE_RX7N	PCIE_TX7P PCIE_TX7N
	PCIE_FTX_C_GRX_P8 N38 PCIE_FTX_C_GRX_N8 M37	PCIE_RX8P PCIE_RX8N	PCIE_TX8P PCIE_TX8N
	PCIE_FTX_C_GRX_P9 M35 PCIE_FTX_C_GRX_N9 L36	PCIE_RX9P PCIE_RX9N	PCIE_TX9P PCIE_TX9N
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	PCIE_FTX_C_GRX_P12 J38 PCIE_FTX_C_GRX_N12 H37	PCIE_RX12P PCIE_RX12N	PCIE_TX12P PCIE_TX12N
	PCIE_FTX_C_GRX_P13 H35 PCIE_FTX_C_GRX_N13 G36	PCIE_RX13P PCIE_RX13N	PCIE_TX13P PCIE_TX13N
	PCIE_FTX_C_GRX_P14 G38 PCIE_FTX_C_GRX_N14 F37	PCIE_RX14P PCIE_RX14N	PCIE_TX14P PCIE_TX14N
	PCIE_FTX_C_GRX_P15 F35 PCIE_FTX_C_GRX_N15 E37	PCIE_RX15P PCIE_RX15N	PCIE_TX15P PCIE_TX15N
	CLOCK	PCIE_REFCLKP PCIE_REFCLKN	
<25> CLK_PEG_VGA <25> CLK_PEG_VGA#	AB35 AA36		
	2 R389 1 VGA@10K_0402_5% AH16	PWRGOOD	CALIBRATION PCIE_CALRPP PCIE_CALRPN
3.3-V tolerant	VGA_RST# AA30 @	PERSTB	



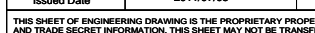
<VARY_BL>
LCD PWM (pulse width modulated)
output to adjust LCD brightness
Active High
External 10-kΩ pull-down recommended.



Link E and link F can only be configured as one DisplayPort link at a time (mutually exclusive).
(eDP is connected to link E.)

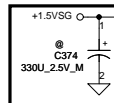


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6V4Z
W6K
3V6M

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R04 Modify BOM



SM010030010

300ma 120ohm@100mhz DCR 0.3

120ohm/0.3A

+1.8VSG

BLM18AG121SN1D_2P

VGA@

Ref137-12-

remove Bead

+3VSG

SM010030010

300ma 120ohm@100mhz DCR 0.3

120ohm/0.3A

+1.8VSG

BLM18AG121SN1D_2P

VGA@

470ohm/1A

SM010030010

200ma 120ohm@100mhz DCR 0.2

+1.8VSG

BLM18AG121SN1D_2P

VGA@

SM010030010

200ma 120ohm@100mhz DCR 0.2

120ohm/0.3A

+1.8VSG

BLM18AG121SN1D_2P

VGA@

+1.0VSG

BLM18AG121SN1D_2P

VGA@

470ohm/1A

SM010030010

200ma 120ohm@100mhz DCR 0.2

120ohm/0.3A

+1.0VSG

BLM18AG121SN1D_2P

VGA@

470ohm/1A

SM010030010

200ma 120ohm@100mhz DCR 0.2

120ohm/0.3A

+1.0VSG

BLM18AG121SN1D_2P

VGA@

470ohm/1A

SM010030010

200ma 120ohm@100mhz DCR 0.2

120ohm/0.3A

+1.0VSG

BLM18AG121SN1D_2P

VGA@

470ohm/1A

SM010030010

200ma 120ohm@100mhz DCR 0.2

120ohm/0.3A

IREF

MEM I/O

AC7

VDDR#1#1

AC10

VDDR#1#3

AC10

VDDR#1#4

AC10

VDDR#1#5

AC10

VDDR#1#6

AC10

VDDR#1#7

AC10

VDDR#1#8

AC10

VDDR#1#9

AC10

VDDR#1#10

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VDDR#1#20

AC10

VDDR#1#21

AC10

VDDR#1#22

AC10

VDDR#1#23

AC10

VDDR#1#24

AC10

VDDR#1#25

AC10

VDDR#1#26

AC10

VDDR#1#27

AC10

VDDR#1#28

AC10

VDDR#1#29

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VDDR#1#30

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VDDR#1#31

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VDDR#1#32

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VDDR#1#33

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VDDR#1#34

AC10

VDDR#1#35

AC10

VDDR#1#36

AC10

VDDR#1#37

AC10

VDDR#1#38

AC10

VDDR#1#39

AC10

VDDR#1#40

AC10

SIC 216-0833000 A11 THAMES XT M2

THA@

VDDR#1#1

VDDR#1#2

VDDR#1#3

VDDR#1#4

VDDR#1#5

VDDR#1#6

VDDR#1#7

VDDR#1#8

VDDR#1#9

VDDR#1#10

VDDR#1#11

VDDR#1#12

VDDR#1#13

VDDR#1#14

VDDR#1#15

VDDR#1#16

VDDR#1#17

VDDR#1#18

VDDR#1#19

VDDR#1#20

VDDR#1#21

VDDR#1#22

VDDR#1#23

VDDR#1#24

VDDR#1#25

VDDR#1#26

VDDR#1#27

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VDDR#1#29

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VDDR#1#31

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VDDR#1#36

VDDR#1#37

VDDR#1#38

VDDR#1#39

VDDR#1#40

VDDR#1#41

VDDR#1#42

VDDR#1#43

VDDR#1#44

VDDR#1#45

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VDDR#1#164

VDDR#1#165

VDDR#1#166

VDDR#1#167

VDDR#1#168

VDDR#1#169

VDDR#1#170

VDDR#1#171

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VDDR#1#177

VDDR#1#178

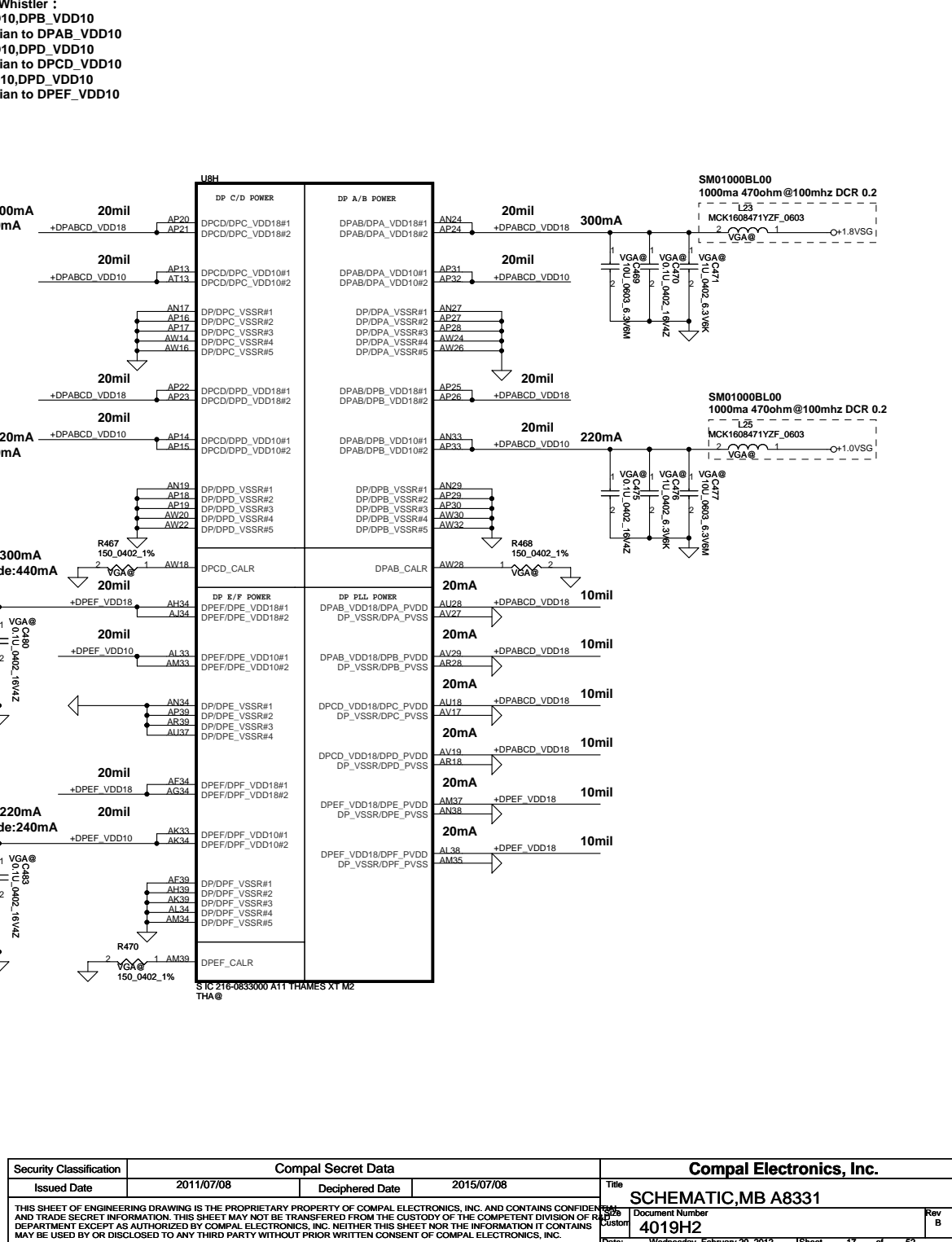
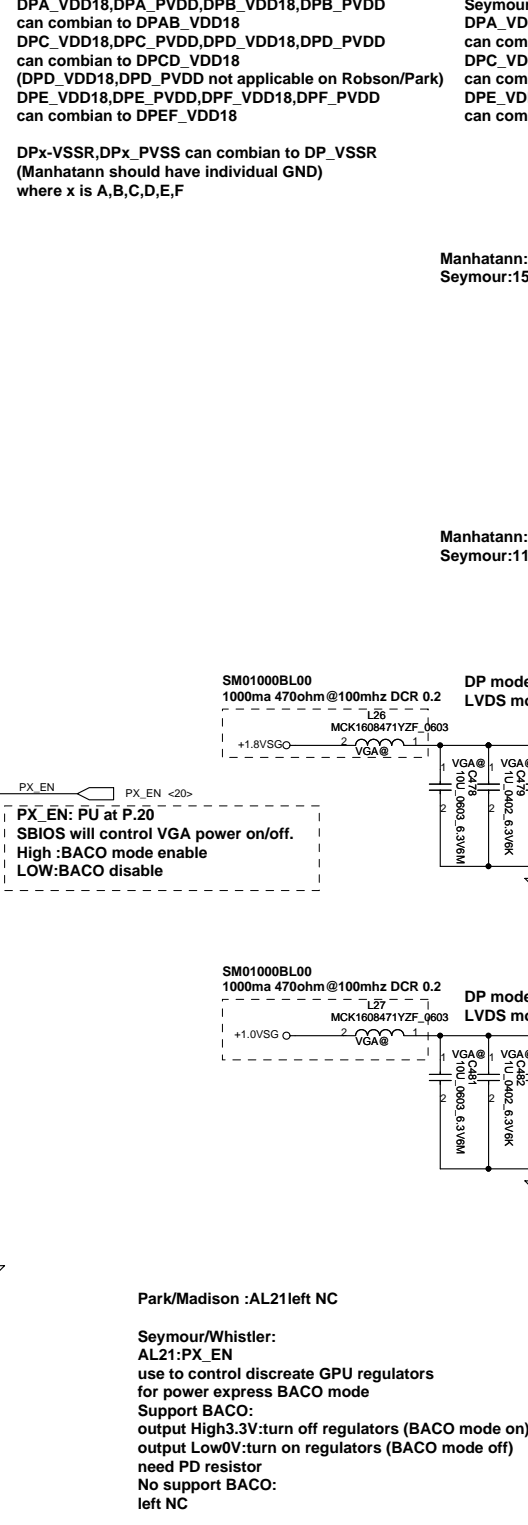
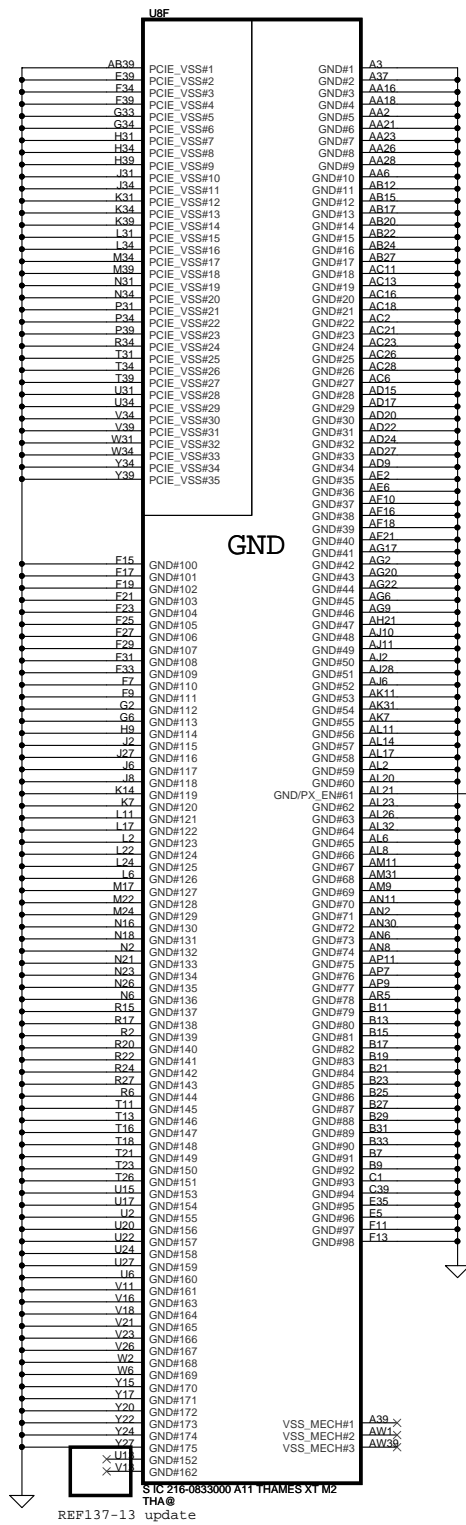
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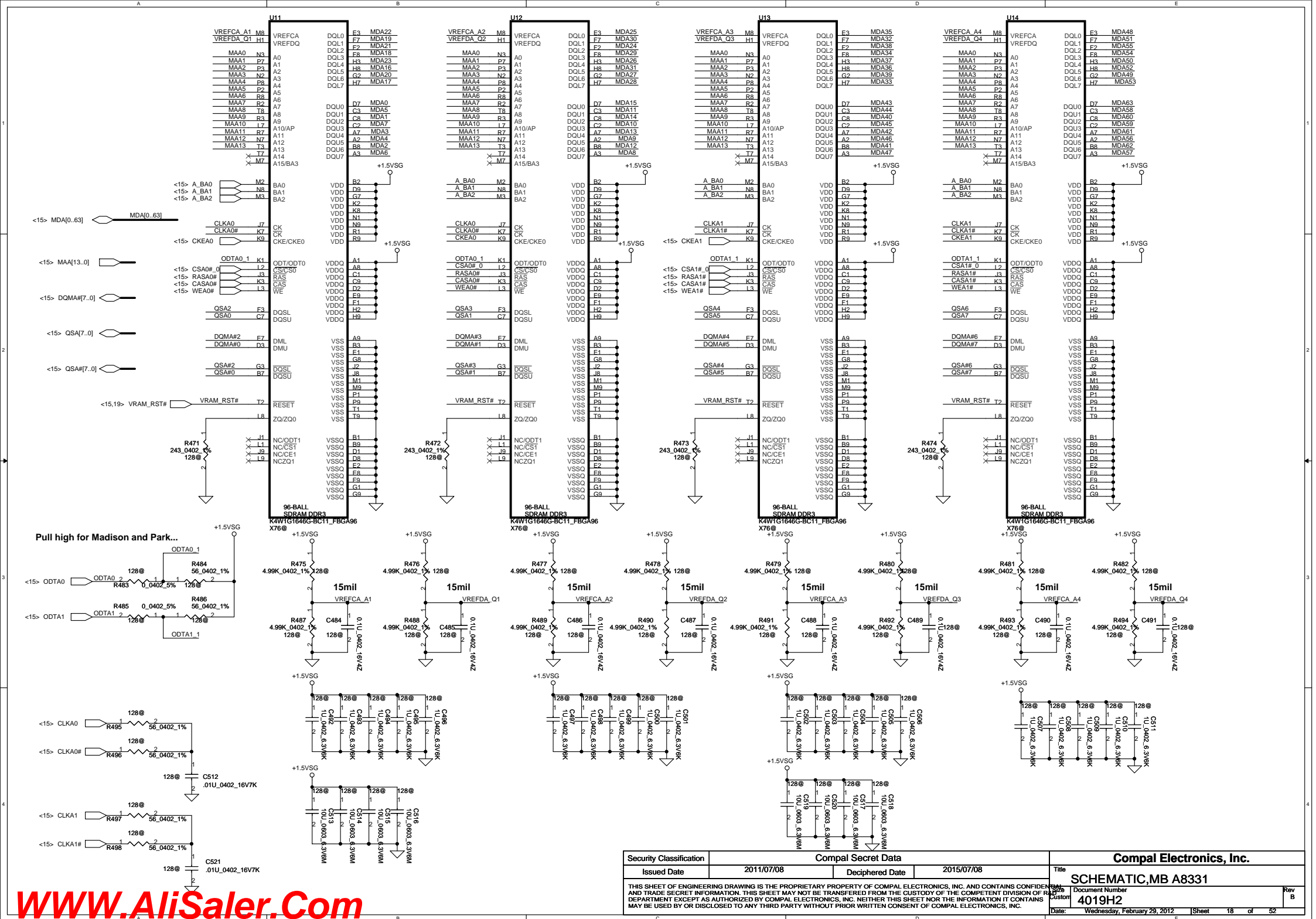
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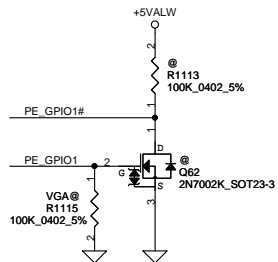
VDDR#1#181

VDDR#1#182

VDDR#1#







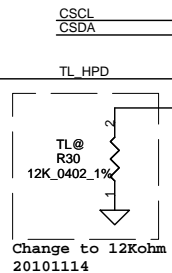
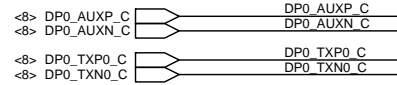
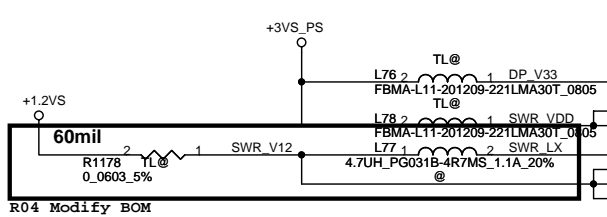
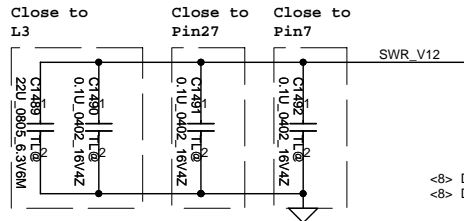
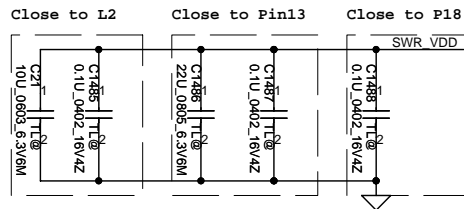
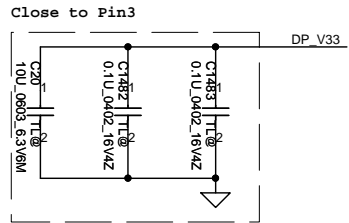
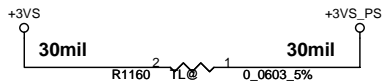
	Dis only	Muxless High performance GPU	Muxless Power-saving GPU
VGA_PWR_ON	1	1	0
1.5_VDDC_PWREN	1	1	0
+3.3VSG	ON	ON	OFF
+1.8VSG	ON	ON	OFF
+1.0VSG	ON	ON	OFF
+VGA_CORE	ON	ON	OFF
+1.5VSG	ON	ON	OFF
+BIF_VDDC	+VGA_CORE	+VGA_CORE	OFF

	Normal mode	BACO mode
PX_EN	0	1
1.5_VDDC_PWREN	1	0
VDDC_EN	1	0
1.0_EN	0	1
+3.3VSG	ON	ON
+1.8VSG	ON	ON
+1.0VSG	ON	ON
+VGA_CORE	ON	OFF
+1.5VSG	ON	OFF
+BIF_VDDC	+VGA_CORE	+1.0VSG

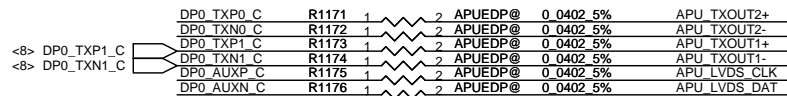
	Graville	Whistler and Seymour
VGA_PWR_ON source signal	INT_VGAPWR_ON	VGA_ON
+3.3VSG	VGA_PWR_ON	SUSP#
+1.8VSG	VGA_PWR_ON	VGA_PWR_ON
+1.0VSG	VGA_PWR_ON	VGA_PWR_ON
+VDDCI	VGA_PWR_ON	Combine with +VGA_CORE
+VGA_CORE	VGA_PWR_ON	1.5_VDDC_PWREN
+1.5VSG	VGA_PWR_ON	1.5_VDDC_PWREN

VGA Power ON Circuit

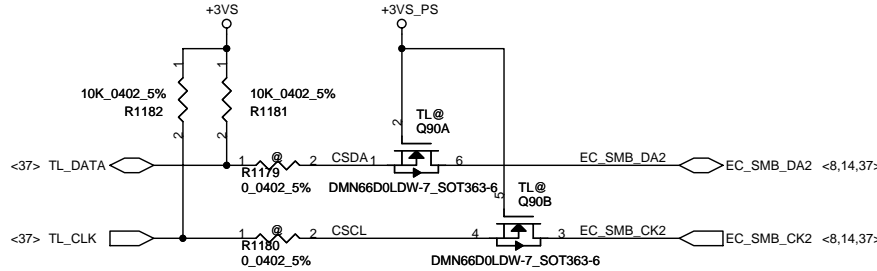
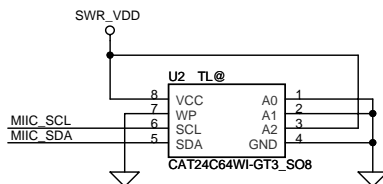
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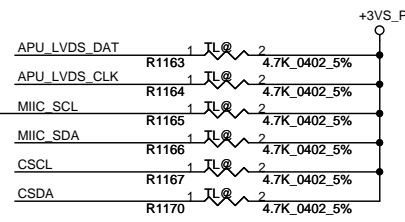
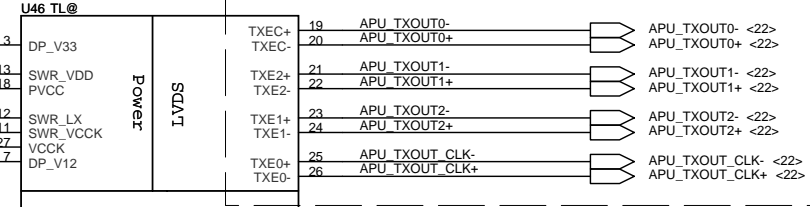
APU Co-lay eDP function



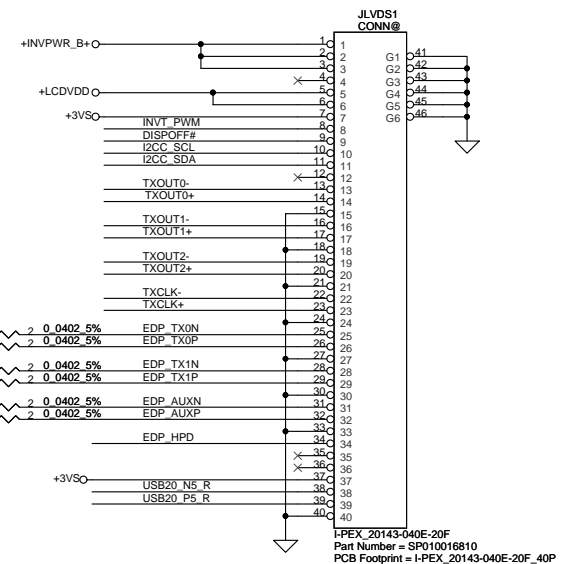
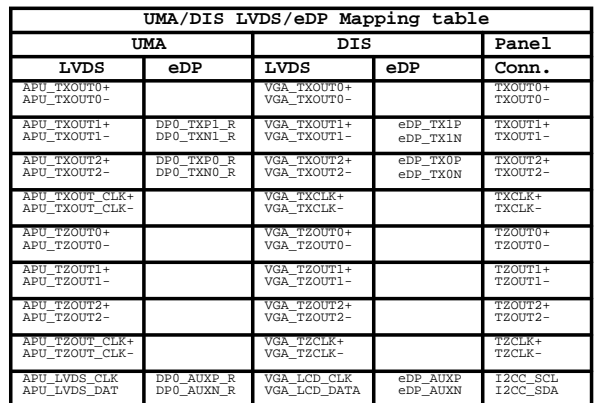
EEROM



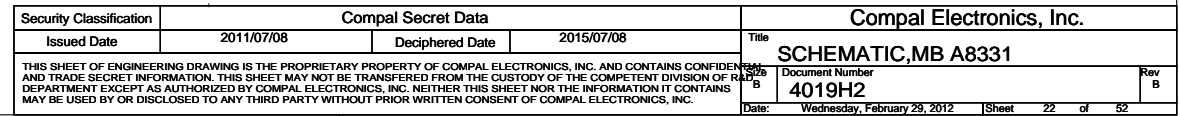
Swap for Meet 40 pin LVDS define (FW Support)

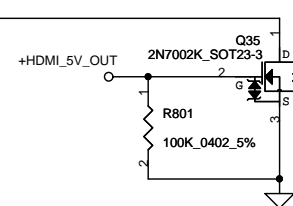
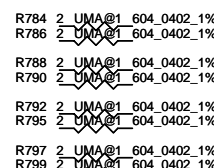
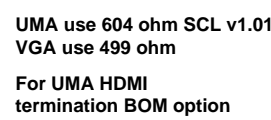
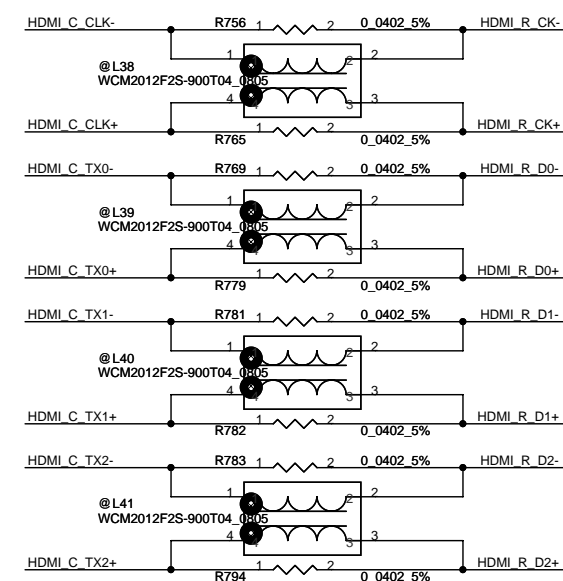
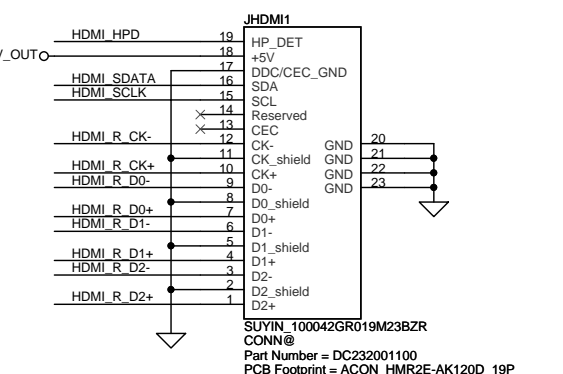


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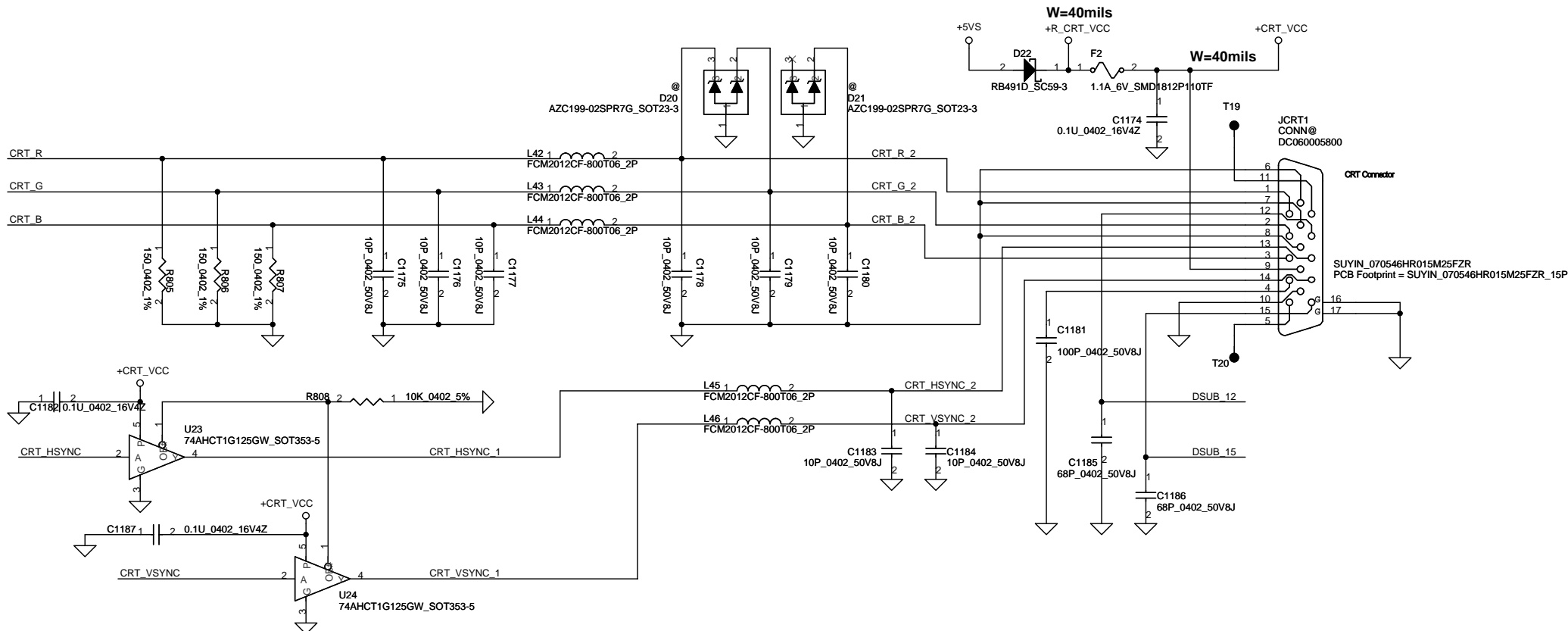


VGA Co-lay eDP function





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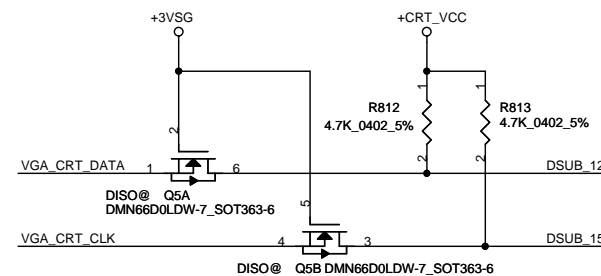
Use common via

From FCH

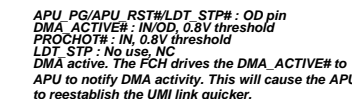
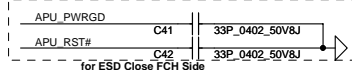
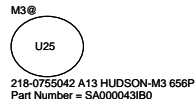
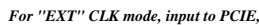
From VGA

<26> FCH_CRT_R	FCH_CRT_R	R809	2	UMA@	1	0.0402_5%	CRT_R
<26> FCH_CRT_G	FCH_CRT_G	R810	2	UMA@	1	0.0402_5%	CRT_G
<26> FCH_CRT_B	FCH_CRT_B	R811	2	UMA@	1	0.0402_5%	CRT_B
<26> FCH_CRT_HSYNC	FCH_CRT_HSYNC	R814	2	UMA@	1	0.0402_5%	CRT_HSYNC
<26> FCH_CRT_VSYNC	FCH_CRT_VSYNC	R815	2	UMA@	1	0.0402_5%	CRT_VSYNC
<26> FCH_CRT_DDC_SDA	FCH_CRT_DDC_SDA	R816	2	UMA@	1	0.0402_5%	DSUB_12
<26> FCH_CRT_DDC_SCL	FCH_CRT_DDC_SCL	R817	2	UMA@	1	0.0402_5%	DSUB_15
<14> VGA_CRT_R	VGA_CRT_R	R818	2	DISO@	1	0.0402_5%	CRT_R
<14> VGA_CRT_G	VGA_CRT_G	R819	2	DISO@	1	0.0402_5%	CRT_G
<14> VGA_CRT_B	VGA_CRT_B	R820	2	DISO@	1	0.0402_5%	CRT_B
<14> VGA_CRT_HSYNC	VGA_CRT_HSYNC	R821	2	DISO@	1	0.0402_5%	CRT_HSYNC
<14> VGA_CRT_VSYNC	VGA_CRT_VSYNC	R822	2	DISO@	1	0.0402_5%	CRT_VSYNC
<14> VGA_CRT_DATA	VGA_CRT_DATA						
<14> VGA_CRT_CLK	VGA_CRT_CLK						

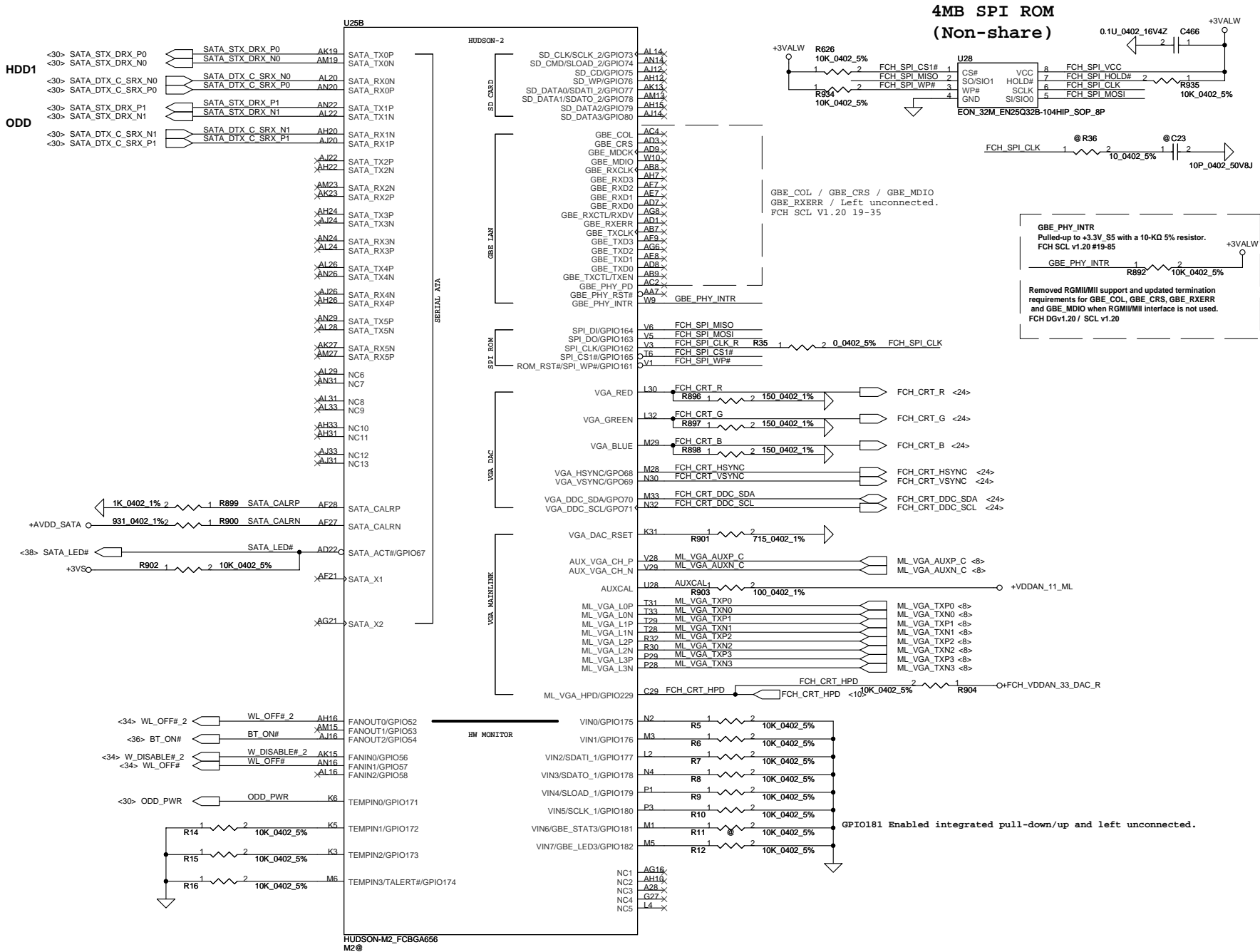
Close to Conn side



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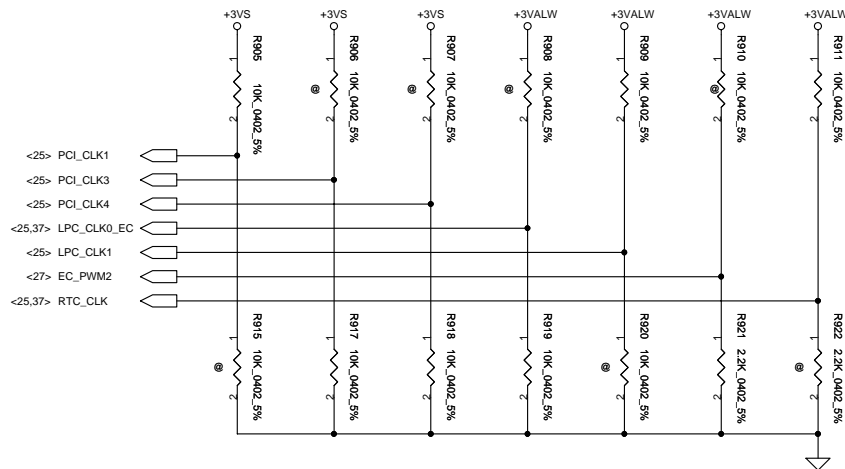


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STRAP PINS

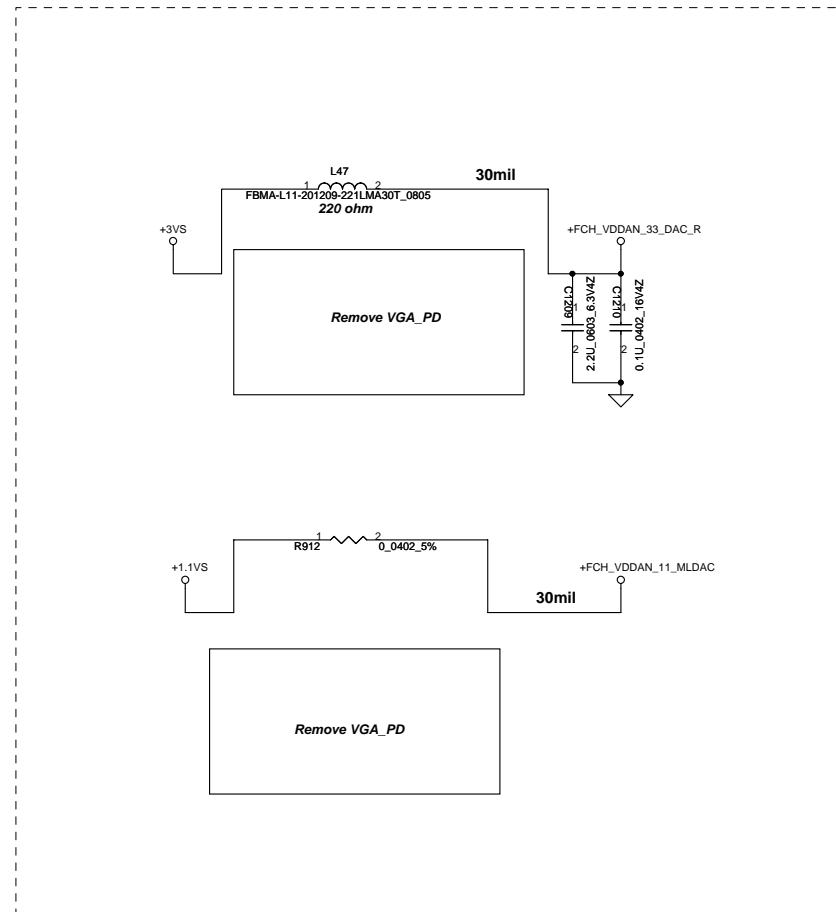
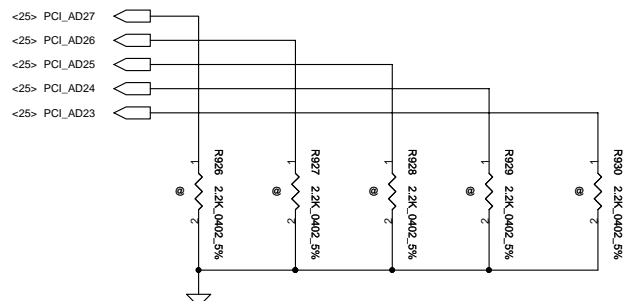
	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED



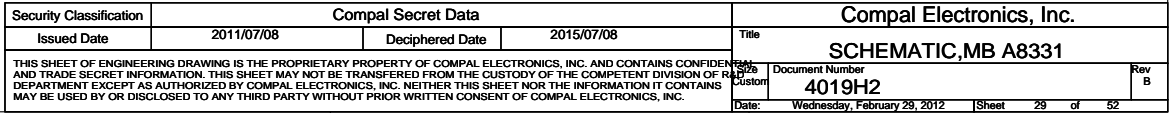
DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

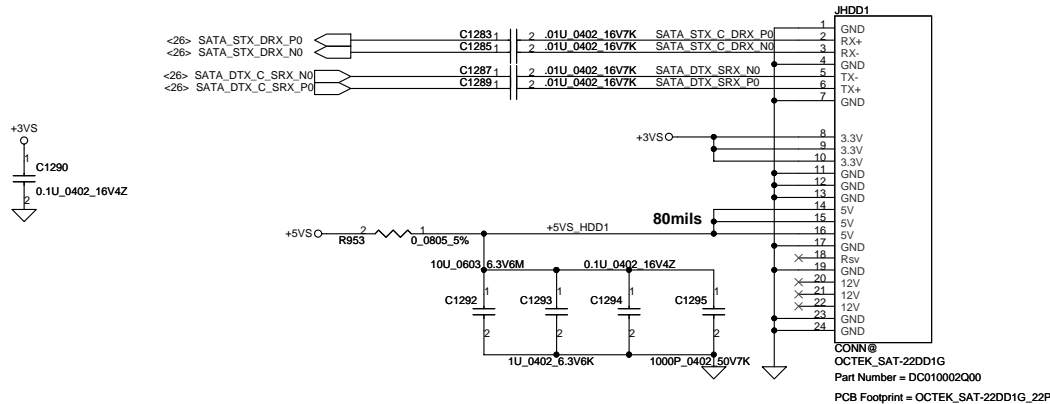
PCI_AD26	PCI_AD27		PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



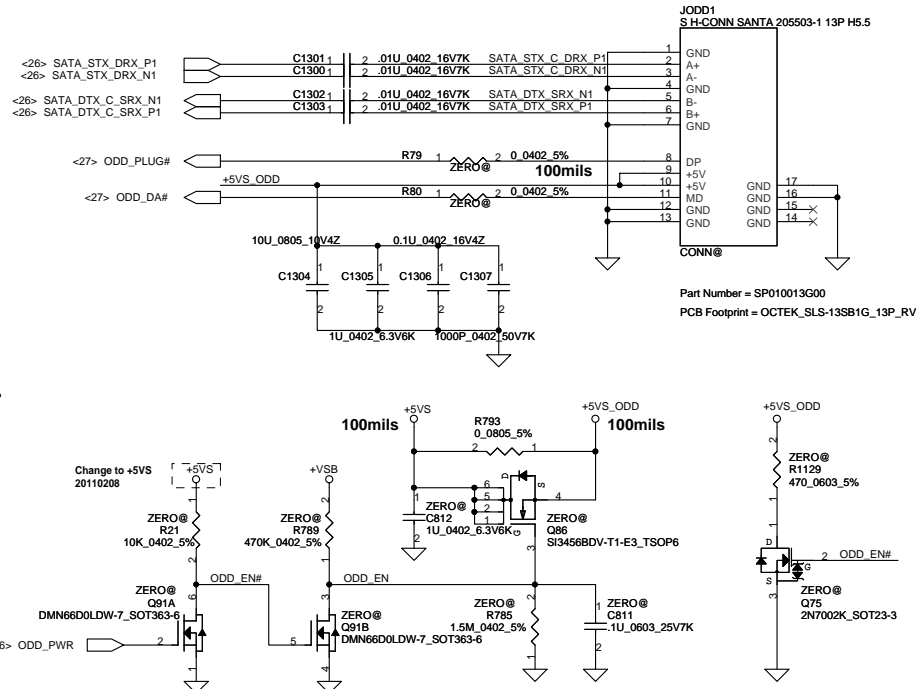
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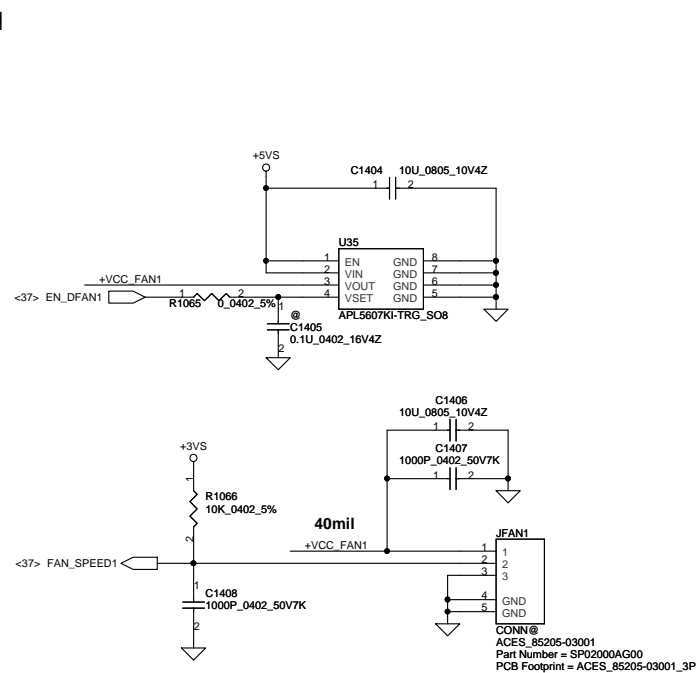
SATA HDD1 Conn.



SATA ODD Conn.

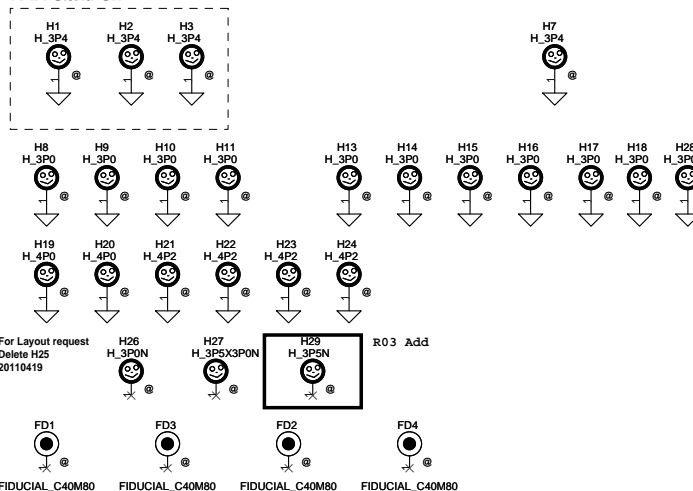


FAN



Screw Hole Follow P5WE0

FAN Stand-Off

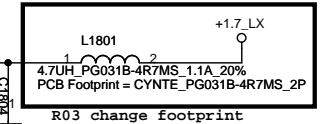


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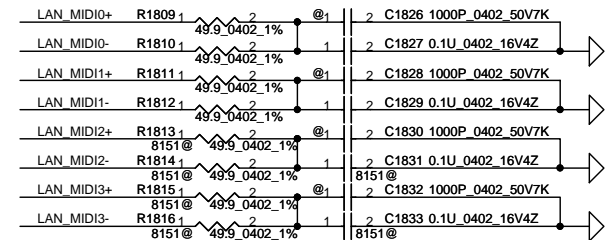
Power On strapping

Pin	Description	Chip Default
LED0	H:Over Clock Enable L:Over Clock Disable * PD 5.1K	H
LED2	H:SWR Switch mode regulator Select * AR8151 Pin23=LED2. AR8152, Pin23 is CLKREQ	--

Place Close to Pin40
DCR< 0.15 ohm
Rate current > 1A

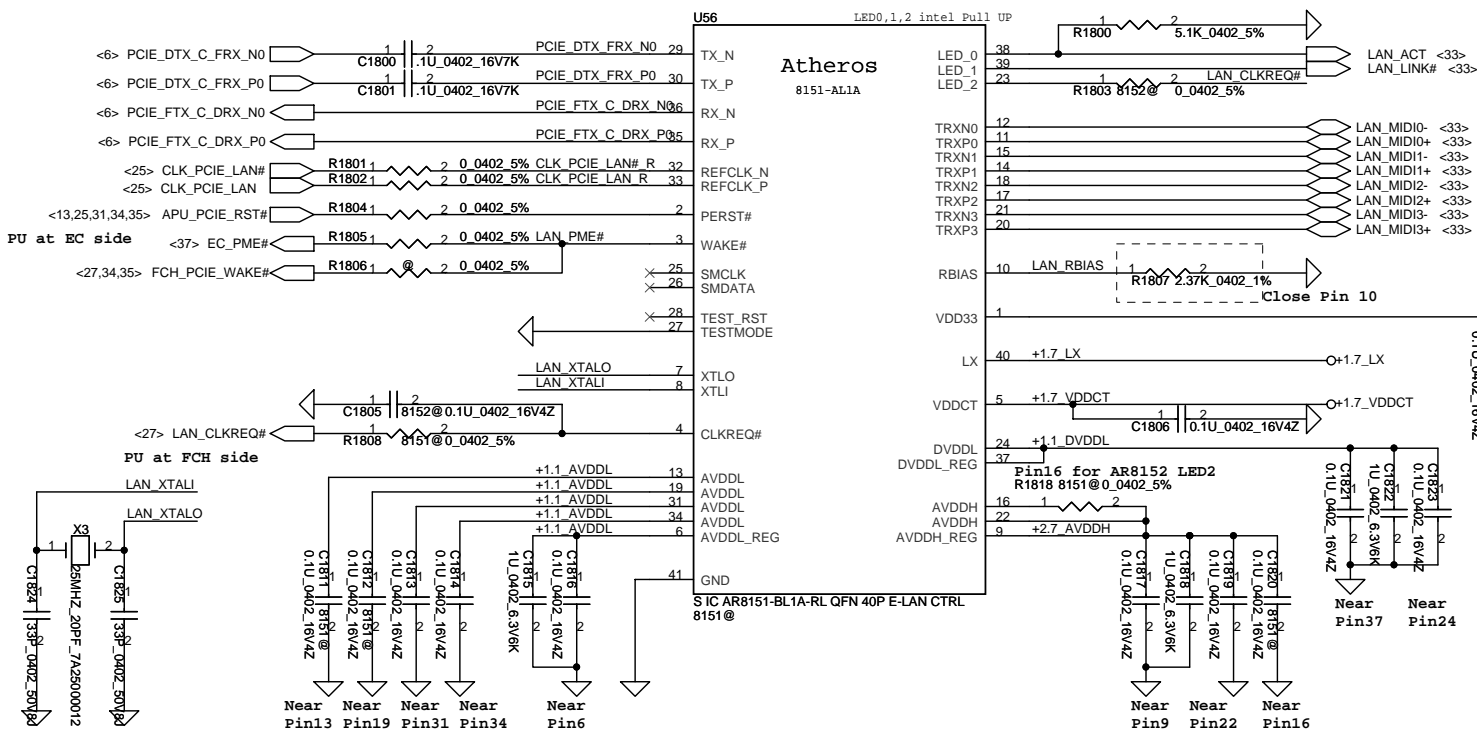


Place Close to LAN chip

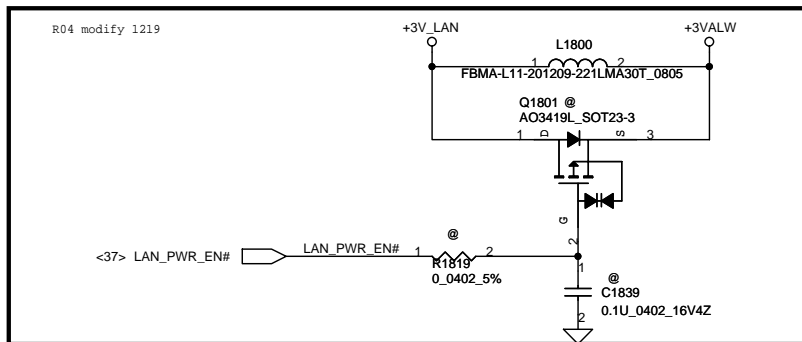


Note 1 : 8152 no mount MDI3+, MDI3-, MDI2-, MDI2+ resistor and cap

Note 2 : C1, C3, C5, C7 reserved for EMI.

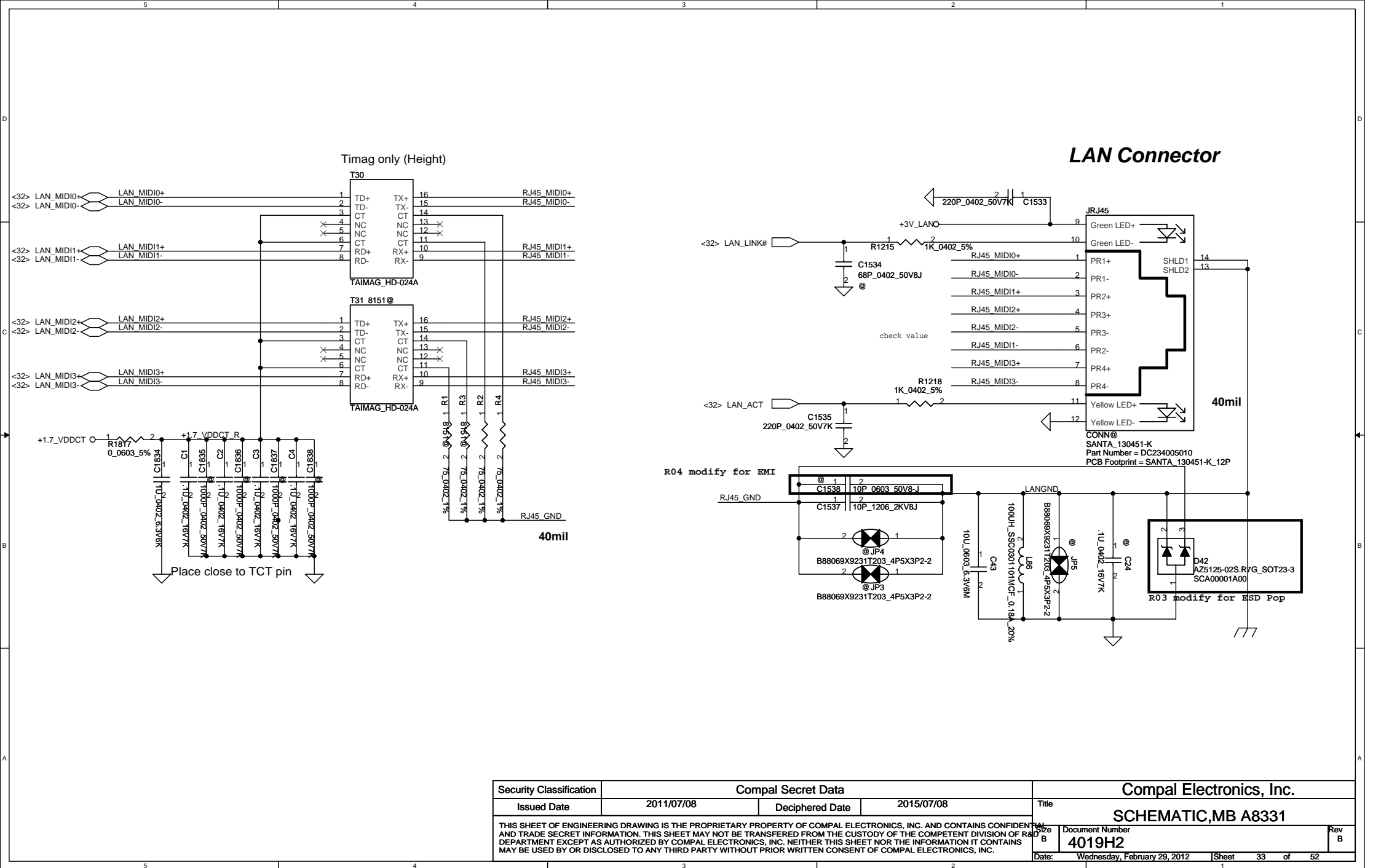


R04 modify 1219

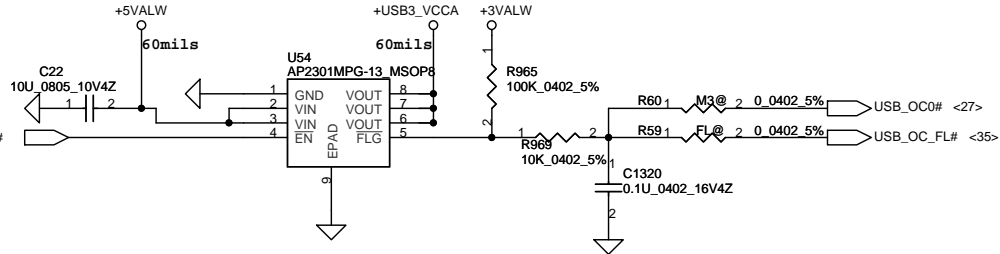
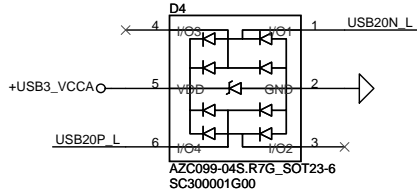
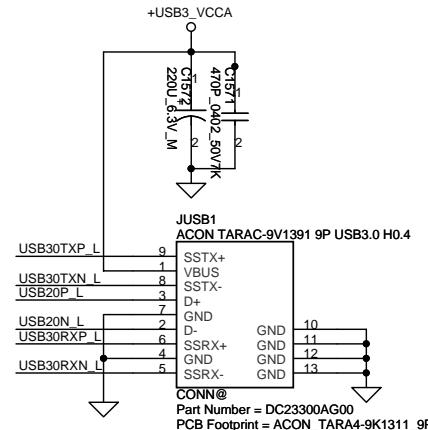
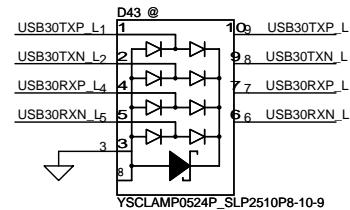
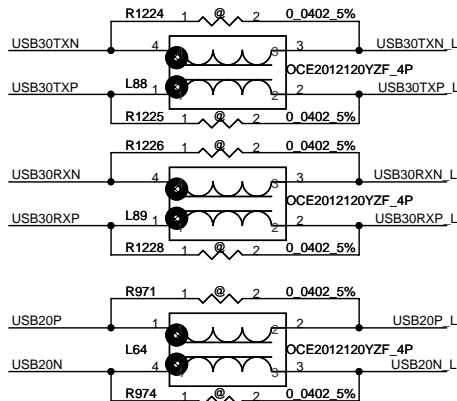
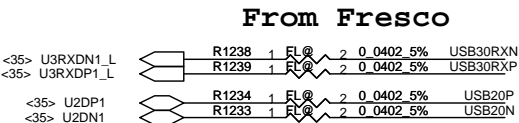
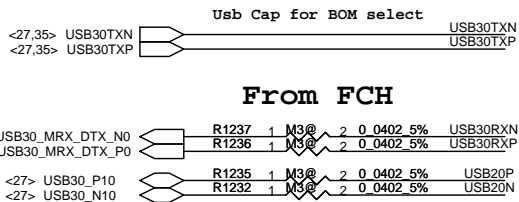


	Pin4	Configure		Pin23	Configure
AR8152	VDDCT_REG		*	CLKREQn	*
AR8151	CLKREQn	*		LED[2]	

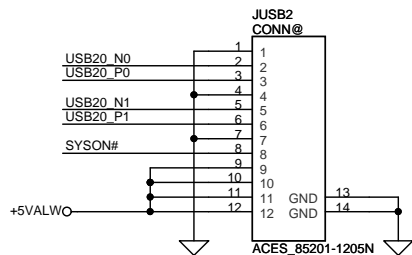
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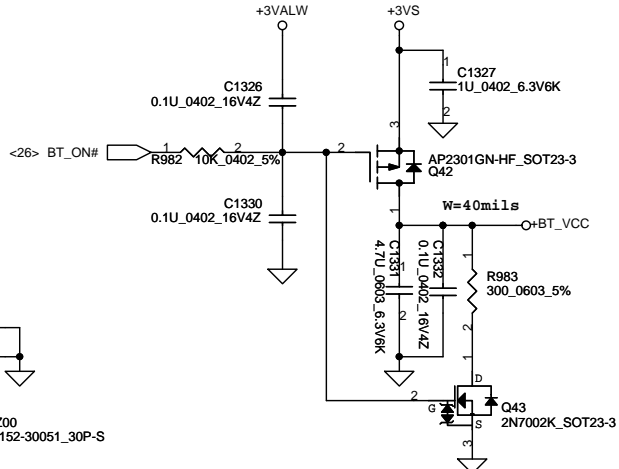
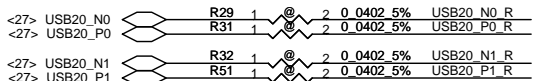
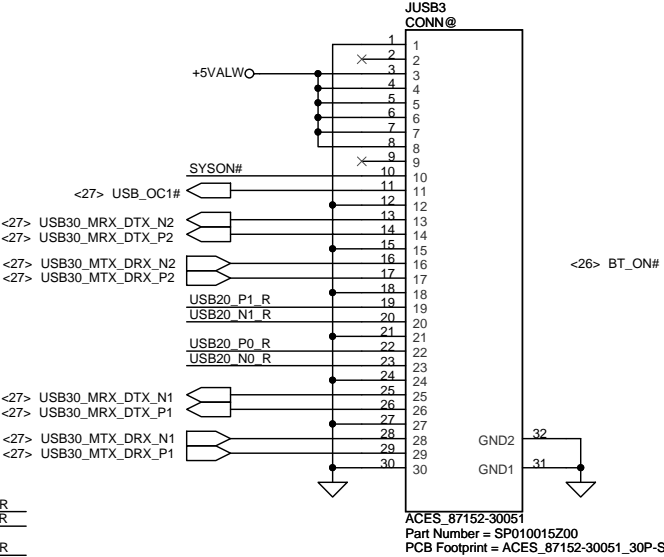
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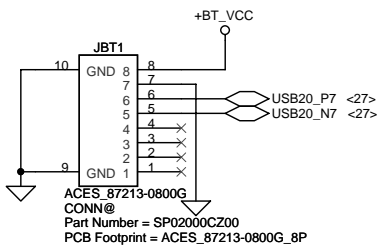
12 Pin USB20/B Conn



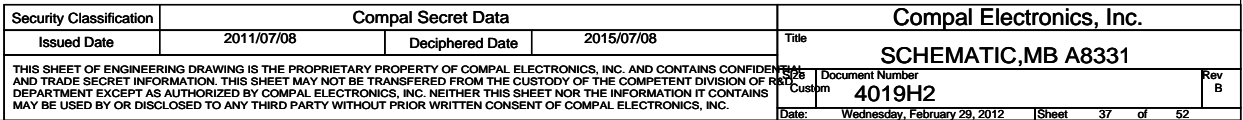
30 Pin USB30/B Zif Conn.



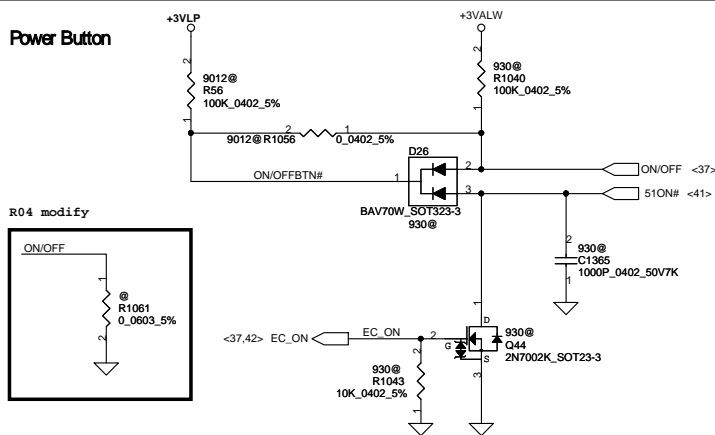
Bluetooth Conn.



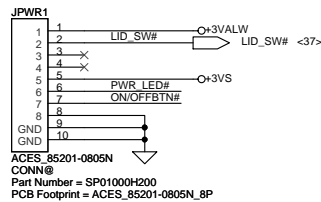
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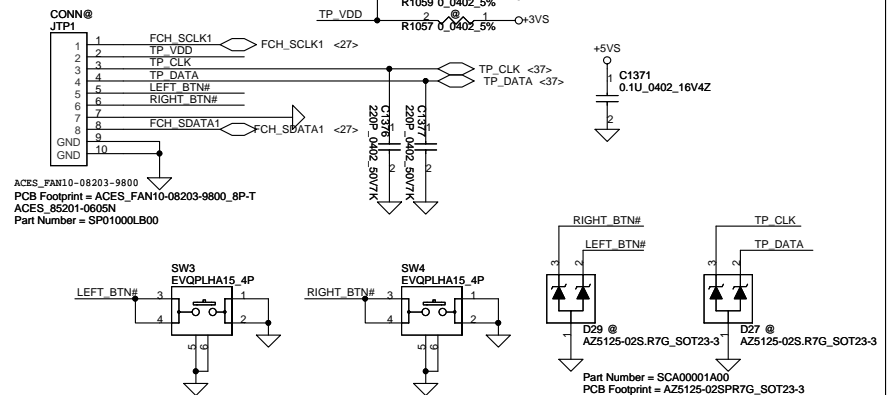
Power Button



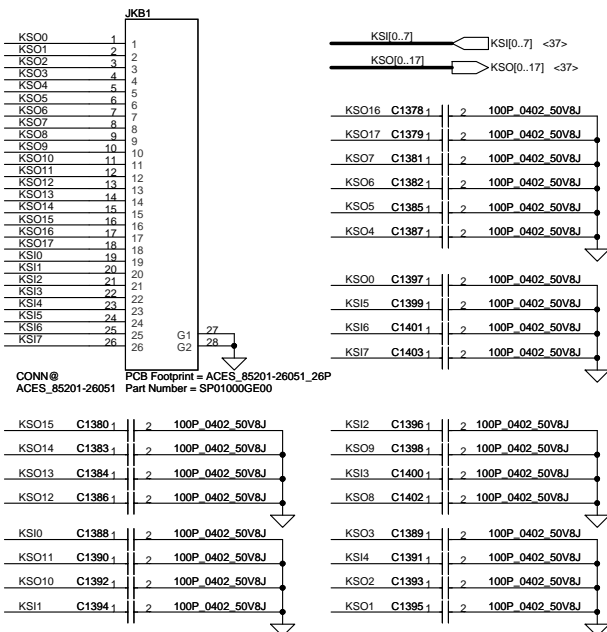
POWER/B



TP Conn.

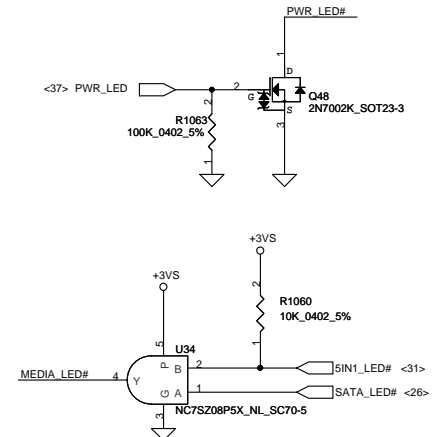
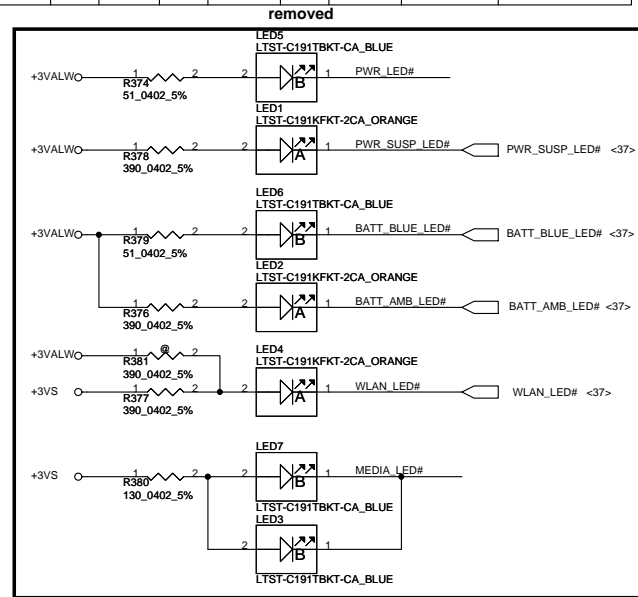


KB Conn.

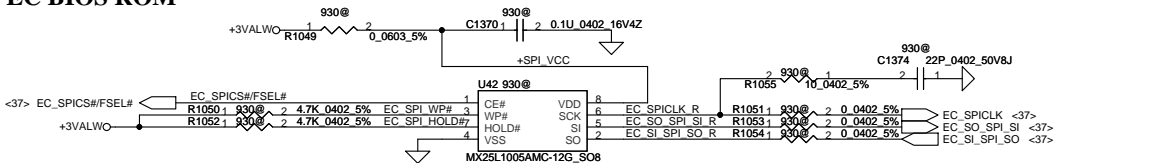


LED

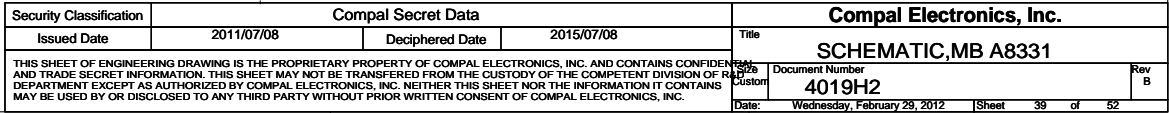
LED Status	Power/SUS		Battery		3G / WLAN		BlueTooth	ACIN
	ON	SUS	Full	Charge	3G	WLAN		
NEW70/80/90	Blue	Amber	Blue	Amber		Amber		



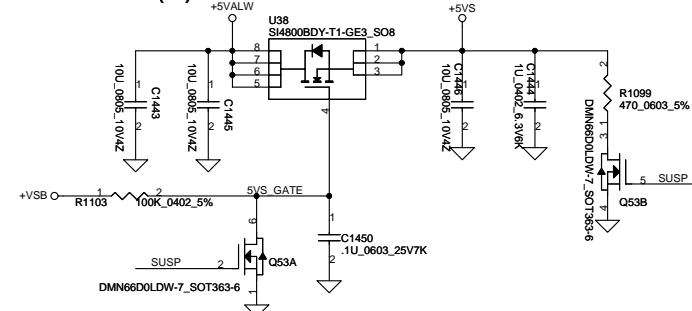
EC BIOS ROM



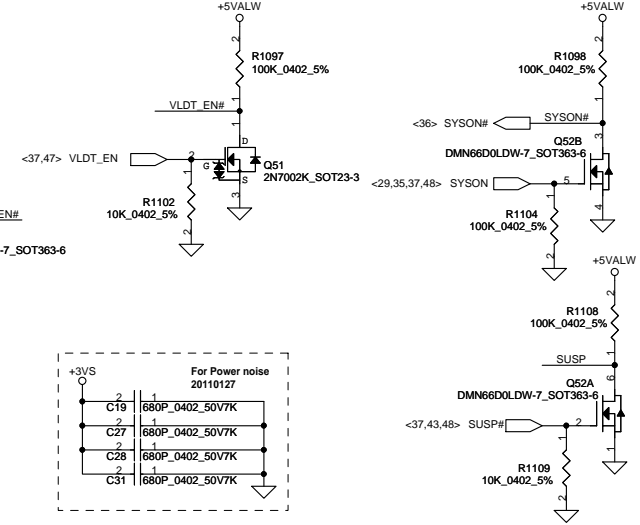
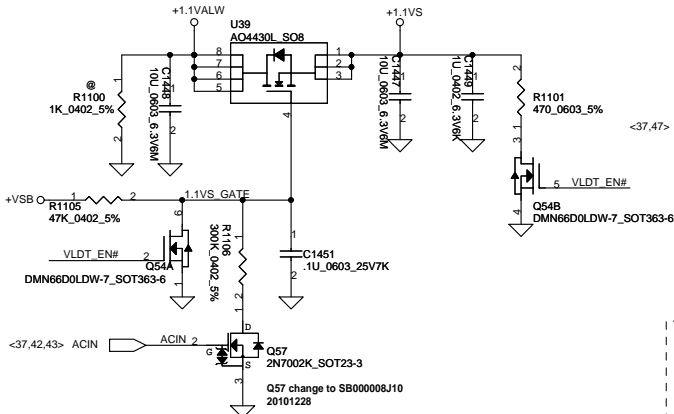
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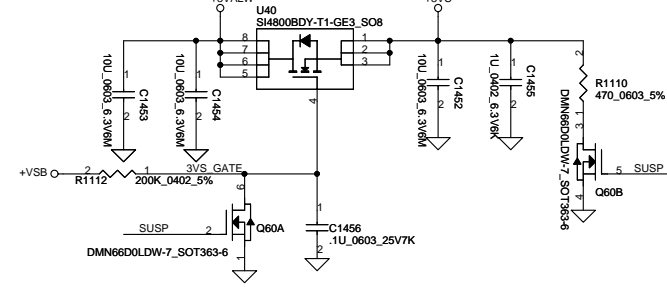
+5VALW TO +5VS (5A)



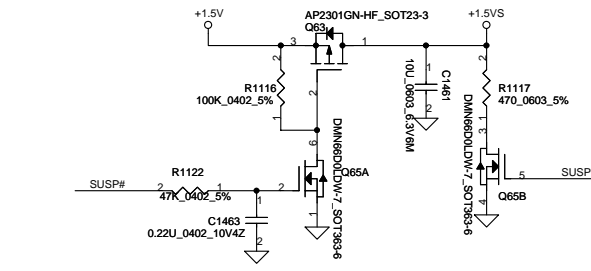
+1.1VALW TO +1.1VS (1.1A)



+3VALW TO +3VS (3.3A)

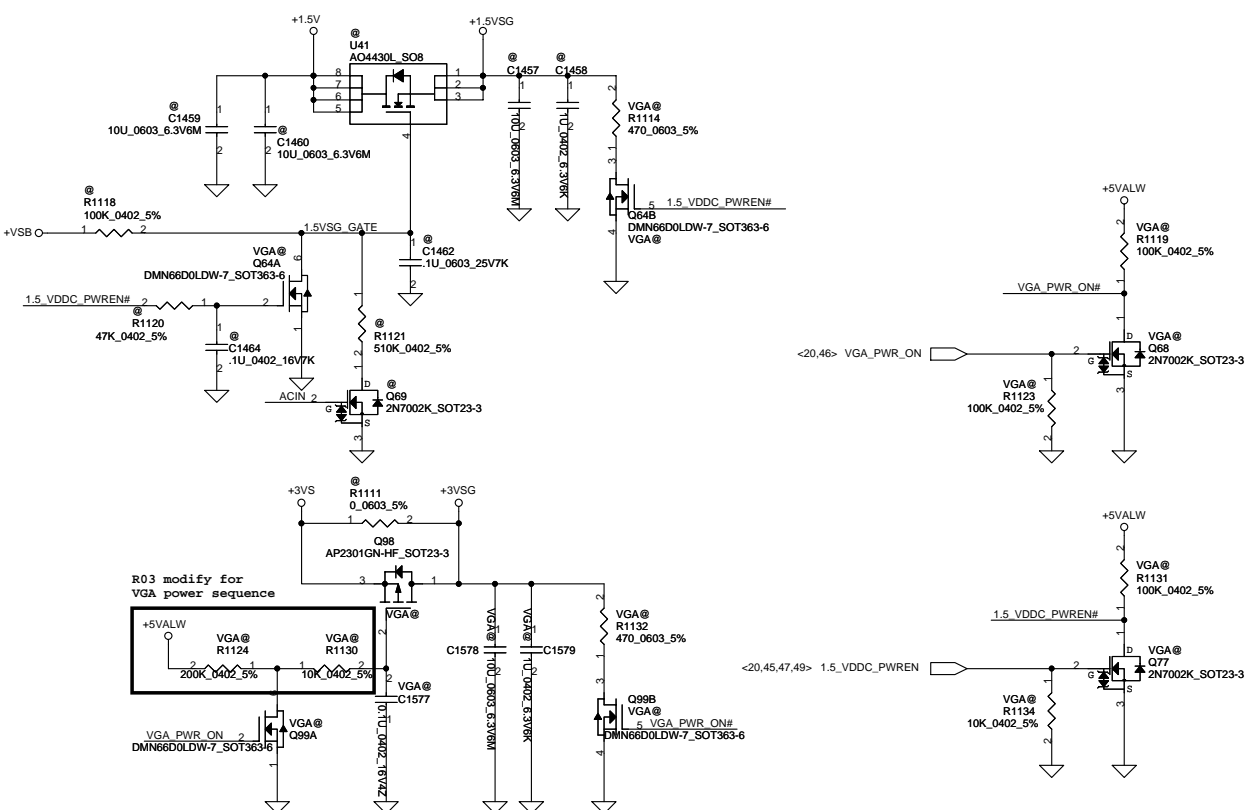


-1.5V TO +1.5VS (1.5A)

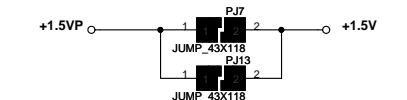
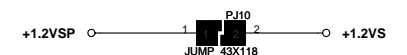
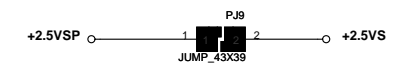
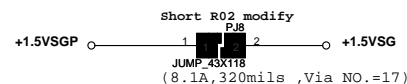
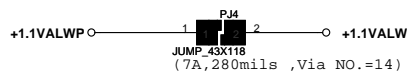
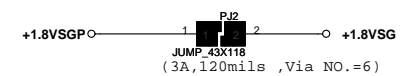
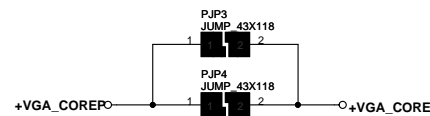
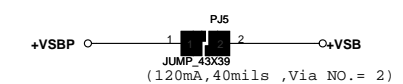
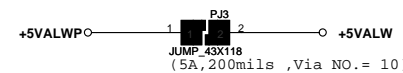
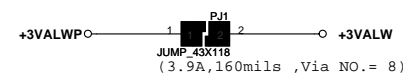
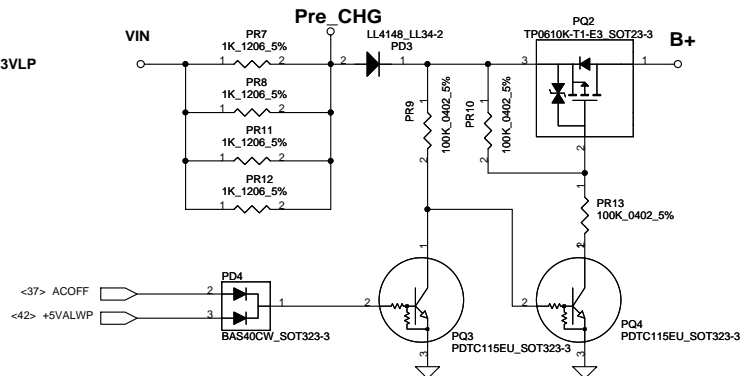
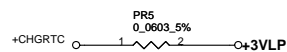
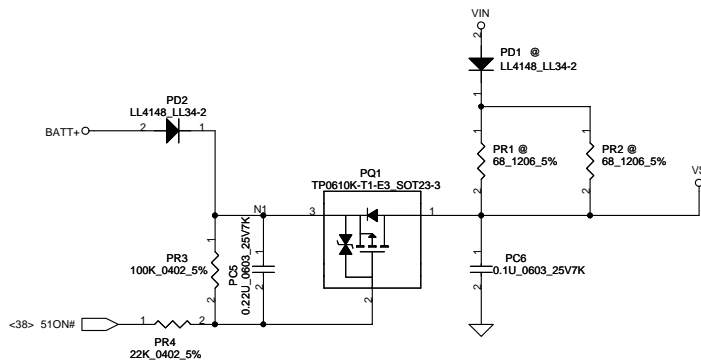
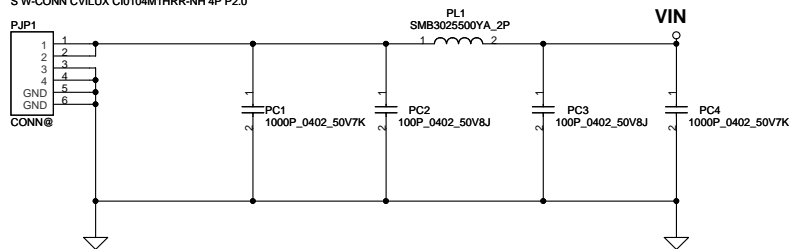


VGA Power

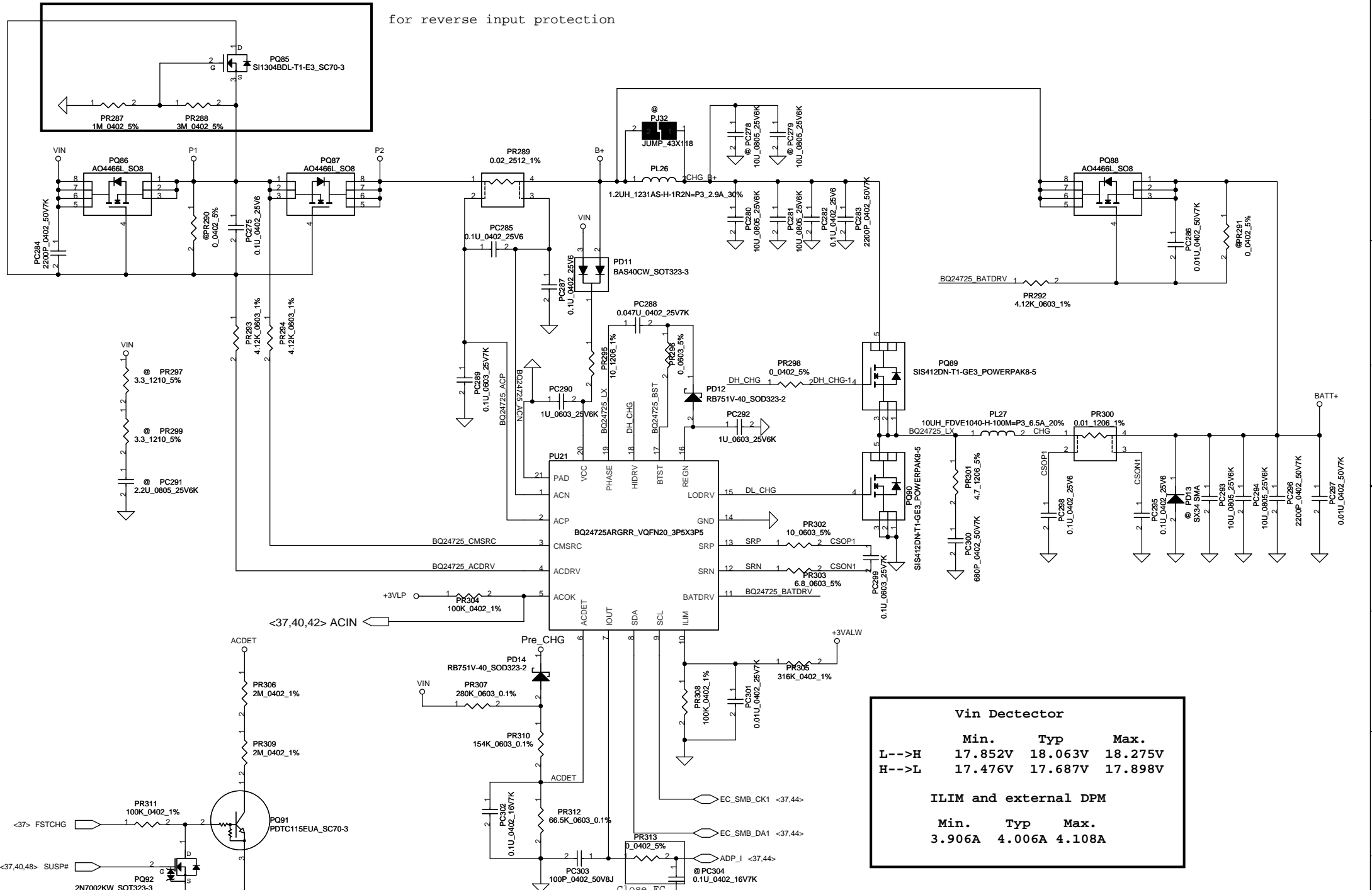
+1.5V to +1.5VSG (1.5A)



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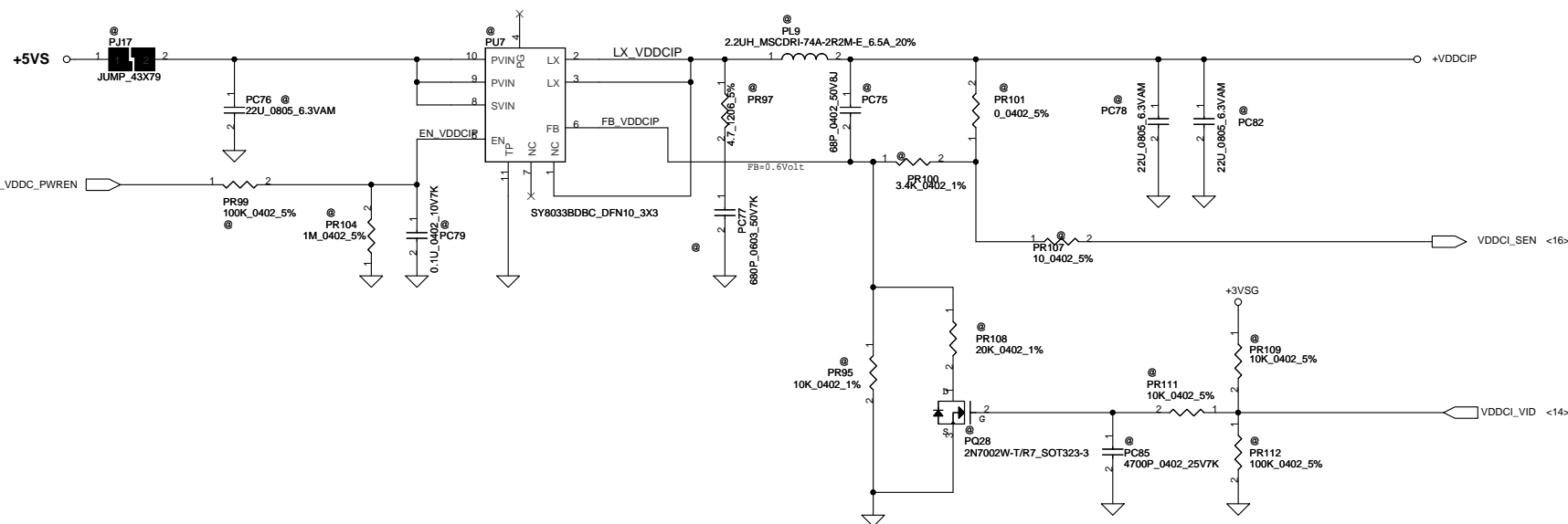




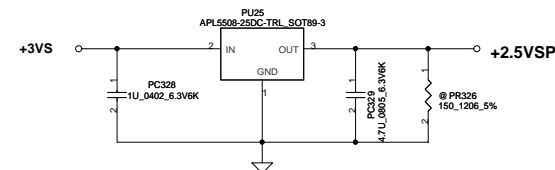
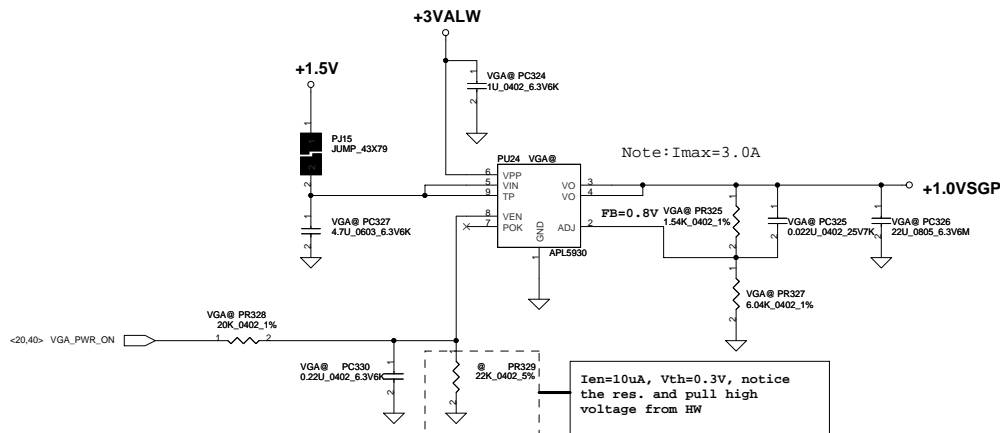
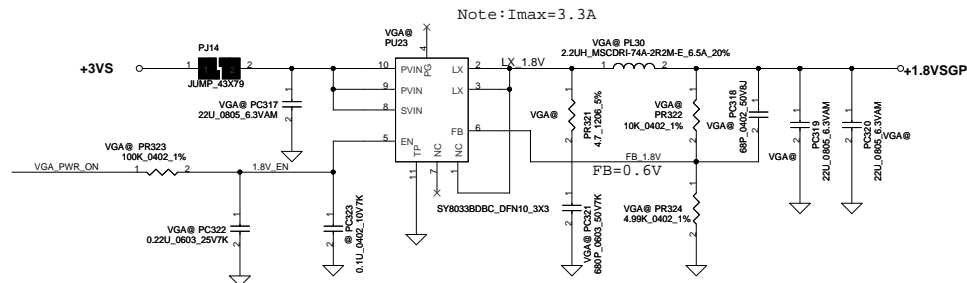
Vin Dectector			
	Min.	Typ	Max.
L-->H	17.852V	18.063V	18.275V
H-->L	17.476V	17.687V	17.898V

ILIM and external DPM			
	Min.	Typ	Max.
	3.906A	4.006A	4.108A

Cesr= 15m ohm
Ipeak= 5.21A Imax= 3.65A Iocp=6.25A
Iocp= 7.7A~11.84A



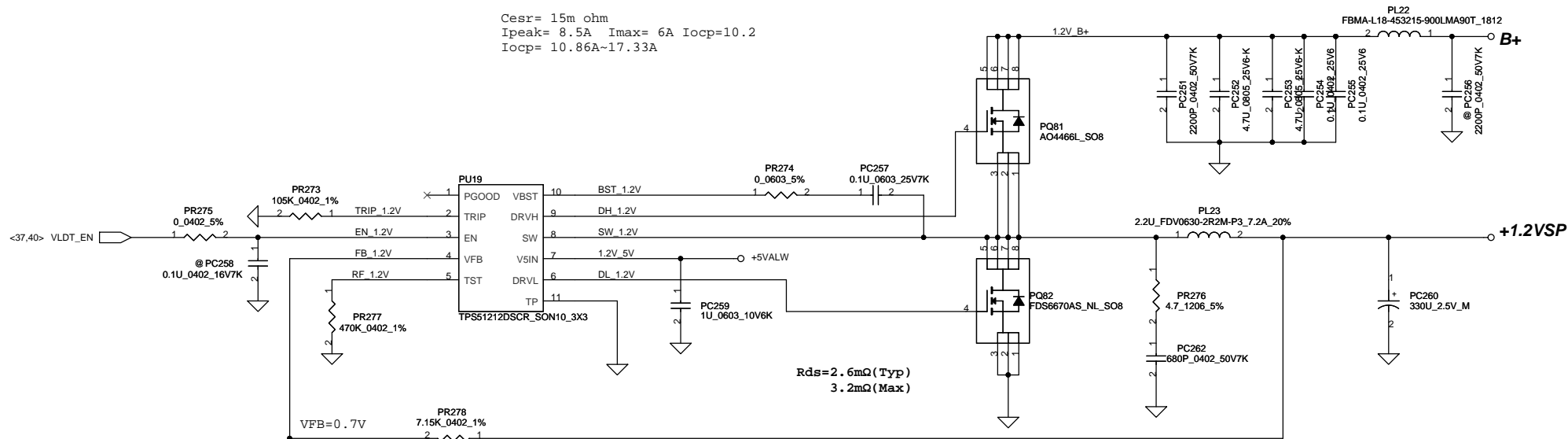
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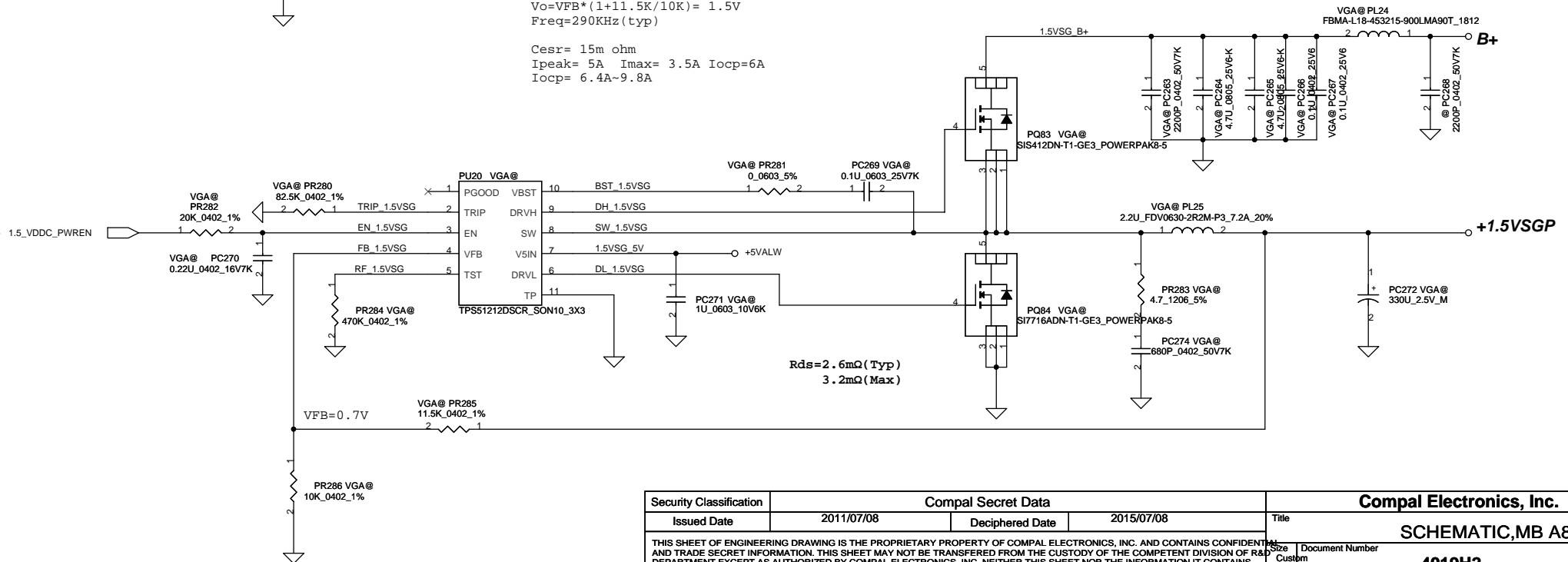
VFB= 0.7V
 $V_o = VFB * (1 + 7.15K / 10K) = 1.2V$
Freq= 266~314KHz , 290KHz (typ)

Cesr= 15m ohm
Ipeak= 8.5A Imax= 6A Iocp=10.2
Iocp= 10.86A~17.33A

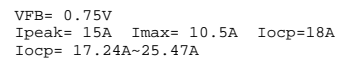


VFB= 0.704V
 $V_o = VFB * (1 + 11.5K / 10K) = 1.5V$
Freq=290KHz (typ)

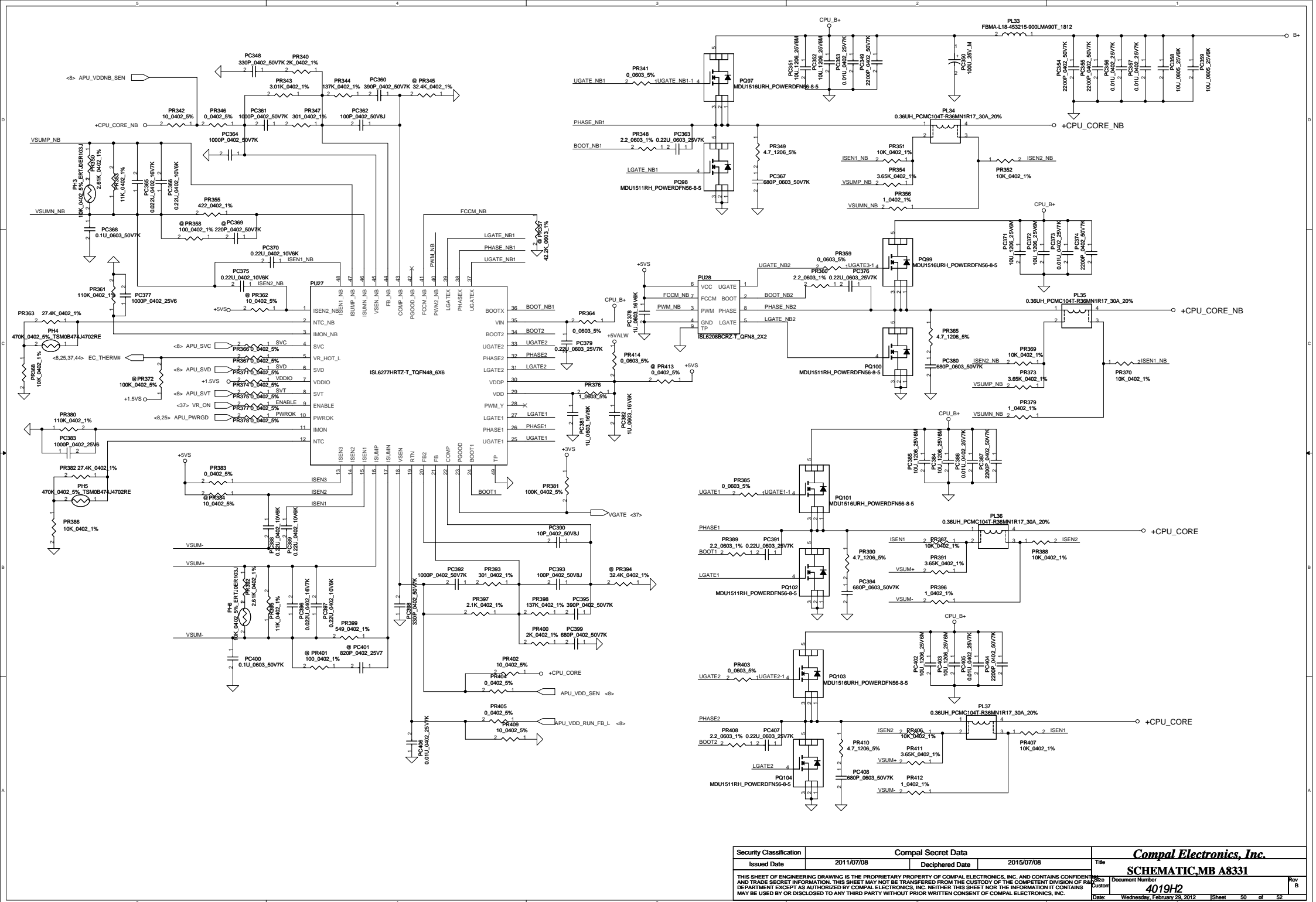
Cesr= 15m ohm
Ipeak= 5A Imax= 3.5A Iocp=6A
Iocp= 6.4A~9.8A



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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1							
2							
3							
4							
5							
6							
7							
8							
9							
10							
11							
12							
13							
14							
15							
16							

Version change list (P.I.R. List)

EVT Stage (0.1~0.2)

- 0817 Pop C1025 180p for VDDIO (SCL v1.02)
Change D16,D17 to SCS00000Z00
- 0818 Change Q50 from BSH138 to BSH111
Unpop R1100 for +1.1VALW
Add D26 BOM Structure for 930@
unpop D4 for USB issue
- 0903 1.Change Card Reader Controller to RTS5209
2.Change LAN to Atheros AR8151
3.Removed D17
- 0904 Add Mini2 Debug Port
- 0905 1.Add Fresco FL1009 USB3.0 Controller
P20. BACO BIFVDDC update
P25. remove Q25 APU power ok
- 0915 1.Remove EC X2
- 0916 1.Add C1361/C1362 10pF for EMI
2.Change D27/D29 footprint to AZ5125
3.Add R402 10k for reserved
4.Add R469/R527 for VGA Internal Thermal Sensor
- 0926 1.Change D4 to SC300001G00 for ESD request
2.Change D33/D34/D37/D40/D41 to SCA00001A00 for ESD request

DVT Stage (0.2~0.3)

- 1.Unpop C954, C955 for Mini2 reserved.
2.Remove R587, R588, Q11 for no need level shift.
3.Pop R469, R527
Unpop U9, R391, C352, C324
for VGA Internal Thermal Interface.
4.Unpop C374 330uF for Use discrete +1.5VSG circuit.
5.Add R1169 1k for RTS2132 Vender suggestion.
6.Reserved R1177 for option EEPROM.
7.Add R1178 for RTS2132 discrete +1.2VS power.
8.Reserved SMBUS(TL_CLK/TL_DATA) to EC for EEPROM option.
9.Reserved BACO circuit and pop C1105.
10.Change D4, D6 to AZC099 for ESD reserved.
11.Change D20, D21 to AZC199-02SPR7G for ESD reserved.
12.Remove D44, D45 for no need.
13.Change C1211, R837 BOM to TL@.
14.Change JTP1 to 6P/8P co-lay footprint for WIN8.
15.Add SMBUS(FCH_SCLK1/FCH_SDAT1) for JTP1.
16.Reserved GPIO166 for future used.
17.Add H29 for ME update.
18.Add C1719, C1720 10pF for RTD5209 EMI request.
19.Change L1801 footprint.
20.Pop D42 and change to SCA00001A00 for ESD.
21.Change C1537 to 10pF 2KV for EMI/ESD.
22.Unpop C1336, C1337, C1338, C1333, C1334, C1335
for MINI2 Reserved.
23.Modify C1911 always pop for noise reduce.
24.Modify R60 to M3@.
25.Change Board ID to "02" for DVT.
26.Add Q30 for EC_THERM reverse for EC common code.
27.Change 9012_PH2 netname to 9012_VGIN for VC function.
28.Unpop R65 for External OTP.
29.Change L68 +5VS to +VDDA.
30.Chnage R1124 to 200k, R1130 to 10k for VGA Power Sequence.
31.Pop R997 for W/L BT combo card BT ON/OFF
32.Change U28 SPI ROM from MXIC to EON

PVT Stage

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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